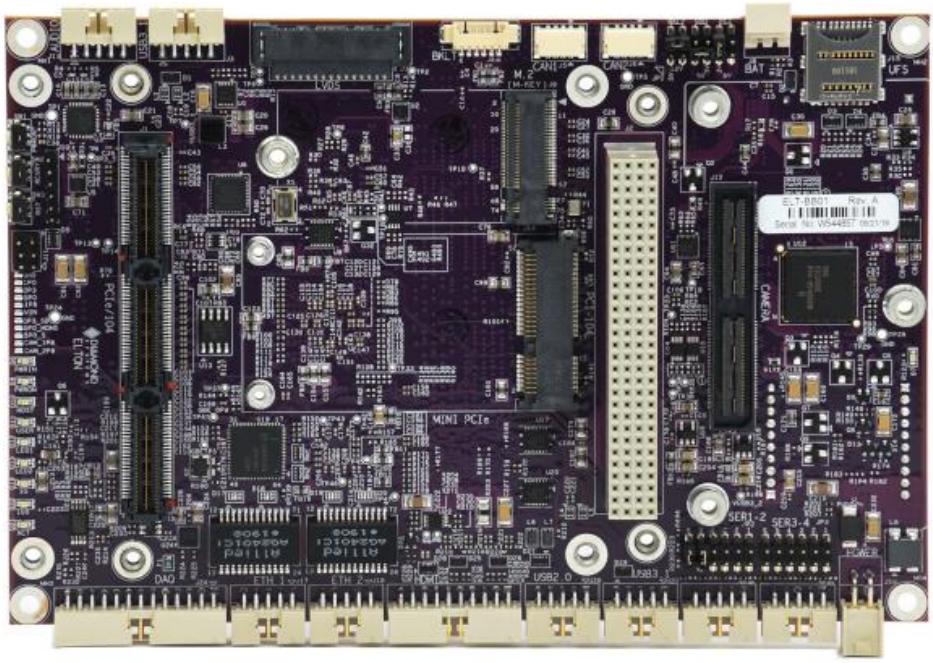
ELTON™

Carrier for NVIDIA® AGX Xavier Module

USER MANUAL



Revision No	Release Date	Comments
1.01	08/05/2019	Initial Release
1.02	01/14/2020	Major Feature Updates
1.03	01/26/2020	Added Sections: PC/10, DAQ, and Getting Started
1.04	03/27/2020	Added Addendum

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Contents

1. IMPORTANT SAFE HANDLING INFORMATION

WARNING!

ESD-Sensitive Electronic Equipment

Observe ESD-safe handling procedures when working with this product.

Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

Diamond Systems boards are designed with complex circuitry and electronic components that are ESD (Electrostatic Discharge)-sensitive. This increases the likelihood of the boards incurring accidental damage during handling, installation, and connection to other equipment.

It is highly recommended that the following precautionary measures and best practices be observed in sequential order:

- Wear an anti-static Wristband/Strap or/and an antistatic Lab Coat or/and Rubber-soled shoes.
- Spread anti-static mats over the table or work surface or/and anti-static mats on the floor.
- Unpack components and remove them from their anti-static bags only when they are ready to be used.
- Avoid ungrounded surfaces such as plastic, carpets, floors, or tables, in the work area.
- Handle boards by the edges and their metal mounting brackets. Avoid touching components on the boards and the edge connectors that connect to expansion slots.

The following information describes common causes of failure found on boards and components returned to Diamond Systems for repair. It is provided as a guideline to avoid accidental damage.

ESD Damage: This type of damage is typically impossible to detect because there is no visual sign of failure or damage. In this type of damage, the board eventually stops functioning because of some defective components. Usually, the failure can be identified and the chip can be replaced.

To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage During Handling or Storage: Physical damage on boards also occur due to mishandling. A common observation is that of a screwdriver slipping on the board during installation, causing a gouge on the PCB surface, cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on components located near the edges. Most Diamond System boards are designed with a minimum 25 mils clearance between the board edge and component pad. The Ground/power planes are located a minimum of 20 mils from the edge to avoid possible shorting from this type of damage. However, these design rules do not prevent damage in all situations.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. Though Diamond Systems boards are resilient to damages, the components located close to the board edges can be damaged or even knocked off the board if the board lies tilted in the rack.

Diamond Systems recommends that all its boards be stored only in individual ESD-safe packaging units. If multiple boards are stored together, they should be contained in bins with dividers placed between the boards. Do not pile boards on top of each other or cram too many boards within a small location. This can cause damage to connector pins or fragile components.

Damage During Installation in a PC/104 Stack: Damage on boards can also occur while installing the board in a PC/104 Stack A common cause of damage occurs when the connector pins are misaligned with their corresponding interfaces on the stack.

For example, during installation, if a PC/104 board pin-mapping is misaligned/shifted by 1 row or 1 column, it can cause the ±12V power and Ground signal lines on the bus to contact the wrong pins on the board and damage components linked to the data bus lines.

Bent Connector Pins: This type of problem can be resolved by re-bending the pins to their original shape using needle-nose pliers.

The most common cause of a bent connector pin is when the board is pulled off a stack by tugging it at angles from one end of the connector to the other, to release it off the stack. Tugging the board off the stack in this manner can bend the pin(s) significantly.

A similar situation can occur when pulling a ribbon cable off a pin header. If the pins are bent too severely, bending them back can cause them to weaken or break. In this case, the connector must be replaced.

Power Damages: There are various causes of power-specific damages that can occur while handling the board. Some common causes such as –a metal screwdriver tip slipping, or a screw dropping onto the board while it is powered-up, causes a short between a power pin and a signal pin on a component.

These faults can cause over-voltage/power supply problems besides other causes described below.

To avoid such damages, assembly operations must be performed when the system is powered off.

Power Supply Wired Backwards: Diamond Systems power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy almost all ICs connected to the power supply. In this case, the board will likely be irreparable and must be replaced. A chip destroyed by reverse or excessive power will often have a visible hole or show some deformation on the surface due to vaporization inside the package.

Overvoltage on Analog Input: If a voltage applied to an analog input exceeds the power specification of the board, the input multiplexer and/or parts behind it can be damaged. Most Diamond Systems boards will withstand an erroneous connection of up to 36V on the analog inputs, even when the board is powered off, but not on all boards, and not under all conditions.

Overvoltage on Analog Output: If an Analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most Diamond boards, a short circuit to Ground on an analog output will deter any damage to the board.

Overvoltage on Digital I/O Line: If a Digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. The acceptable voltage range, on most Diamond Systems boards connected to digital I/O signals is 0-5V, with overvoltage protection up to 5.5V (-0.5 to 5.5V). Overvoltage beyond this limit can damage the circuitry.

Other considerations are Logic Signals, which are typically generated between 12V to 24V.

If a Digital I/O Line of 12V to 24V is connected to a 5V logic chip, the chip will be damaged, and the damage could extend to other chips in the circuit.

IMPORTANT! Always check twice before Powering Up!

2. INTRODUCTION

2.1 Elton Baseboard Overview

The Elton baseboard is the latest product from Diamond Systems to integrate the newly-released Standalone NVIDIA AGX Xavier System on Module (SoM) Series:

- AGX Xavier
- AGX Xavier 8 GB

NOTE: Currently the Elton Board Support Package (BSP) supports the AGX Xavier Module Series only. Support for the AGX Xavier 8 GB Modules will be provided subsequently.

Packaged in an ultra-compact sized form-factor measuring H 6" x W 4" (152.4 mm x 101.6 mm) Elton baseboard is empowered to deliver the latest technologically innovative breakthroughs by converging Fifth Generation (5G) and Fourth Generation (4G) Networking Technologies.

The Elton baseboard integrates the AGX Xavier Series Module to offer a full-featured, embedded system that significantly enhances performance, power efficiency, and optimized I/O capabilities, for processing real-time Artificial Intelligence (AI), Machine and Deep Learning and high-level Audiovisual (AV) computing tasks at unconventional speeds.

Feature Description and Connector Type

Feature	***Description***	***Connector Type***
Power	9V-20V Wide Input Supply Range	2x2 Samtec IPL1
USB Interfaces	2x USB 2.0	2x5 Header
	2x USB 3.1	2x5 Header (x2)
Ethernet Controllers	10/100/1000 Mbps through I210 Controller with On-board Magnetics	RJ45 GbE 2x5 Header
	10/100/1000 Mbps through RGMII Interface to KSZ9031 PHY with On-board Magnetics	RJ45 GbE 2x5 Header
Mass Storage	1 MINI-PCI EXPRESS (mPCIe) Socket	RA PCIe MiniCard 52 Position (52-Pin-Card-Edge-Type Connector)
	1 M.2 PCIe SSD Socket 2242 (22mm wide x 42mm long)	M.2 Socket
	1 Universal Flash Storage (UFS) and Micro SD	UFS & Micro SD Push-Pull Type Connector
Expansion Connections	PCIe/104 3-Bank (4Nos x1 PCIe, 2x USB 2.0, 1No x8 PCIe)	156 POS SMT Mezzanine
	PCI-104 via PCIe to PCI Bridge	PCI 104 Press-Fit Connector
Audio Interface	Via SGTL500 CODEC	2x5 Header
Serial Ports	4 RS-232/422/485 Ports. Software configurable through SP336 Transceivers	2x5 Header (x2)
Display Connectors	1 HDMI 2.0a/b Routed from the Module	2x10 Header
	1 Dual-Channel eDP to LVDS and Backlight	2x15 Header
Camera Interface	4 x4 / 8 x2 Lane CSI-2 Camera Interface	2 x 6 0 Receptacle SMT
Data Acquisition (DAQ)	6x SE ADC Input / 3x DE ADC Input to SAM Controller 2x DAC via SAM Controller	2x13 Header
Digital I/Os	13 Digital I/O via SAM Controller	
CAN Header	2x CAN	1x4 1.25mm SMD
Utility Connectors	PWR_BTN, RESET, FORCE RECOVERY	2x3 Header

Operating System Support	
Linux Kernel version 4.4.38; Ubuntu 16.04 AArch64	
Mechanical, Electrical, and Environmental Properties	
Form-Factor	H 6” x W 4” (152.4 mm x 101.6 mm)
Cooling Mechanism	Conduction Cooling
Power Input Range	+9V to +20V
Operating Temperature Range	-25°C to +80°C Ambient

2.2 Elton Baseboard Models

Elton baseboard variants offer a complete modular platform in compliance with requisite specifications that support a wide range of interface options such as board-to-board (B2B) connectors for I/O peripherals, built-in microcontroller, memory, Ethernet, USB, UART, mini-PCI Express interfaces – designed for end-user customization

The Elton Group includes three variants which are listed in the following table. All variants incorporate the same functionalities and differ only in feature requirements.

Model	***Feature***	
ELT-BB01	PCIe/104	✓
ELT-BB02	PCIe/104, and PCI-104	✓
ELT-BB03	PCIe/104, and PCI-104	X

2.3 AGX Xavier Modules Overview

Measuring L x 3.93” X W 3.42" X H 0.62" (100 mm x 87 mm x 0.02 mm) the AGX Xavier and AGX Xavier 8 Series are autonomous, highly sophisticated, low-powered modules, engineered to process more than 32 and 20 trillion operations per second respectively, at a speed of 56 Gbit per second.

Embedded with 9 billion Transistors and a 699 Neuro-Mezzanine Pin Board-to-Board connector that supports Hi-Speed I/O processing of data including PCI/PCIe Gen 5 and Gen 4 technologies, the modules enable Deep Learning Applications to operate in Small Form-Factor (SFF) products such as Computer-on-Module (COMs), and Smart devices such as Cameras, within a secure and automotive environment.

The circuitry and I/O connectors on the baseboard utilize all available features of the AGX Xavier Series Module to deliver highly versatile performance in industrial environments.

AGX Xavier Series Feature Description

Feature	*Description*	
	AGX XAVIER	***AGX XAVIER 8 GB***
GPU	512-core NVIDIA Volta™ GPU with 64 Tensor Cores	384-core NVIDIA Volta™ GPU with 48 Tensor Cores
DL Accelerator	(2x) NVIDIA Deep Learning Accelerator (NVDLA) Engines	(2x) NVIDIA (NVDLA) Engines
CPU	8-core ARMv8.2 @ 64-bit CPU, 8 MB L2 + 4 MB L3	6-core Arm®v8.2 64-bit CPU, 6 MB L2 + 4 MB L3
Memory	16 GB 256-bit LPDDR4x | 136.5 GB/s	8 GB 256-bit LPDDR4x | 85.3 GB/s
Video Encode	2x 1000MP/sec 4x 4K @ 60 (HEVC) 16x 1080p @ 60 (HEVC) 32x 1080p @ 30 (HEVC)	2x 464MP/sec 2x 4K @ 30 (HEVC) 6x 1080p @ 60 (HEVC) 14x 1080p @ 30 (HEVC)
Video Decode	2x 1500MP/sec 2x 8K @ 30 (HEVC) 6x 14k @ 60 (HEVC) 26x 1080p @ 60 (HEVC) 72x 1080p @ 30 (HEVC)	2x 690MP/sec 2x 4K @ 60 (HEVC) 12x 1080p @ 60 (HEVC) 32x 1080p @ 30 (HEVC)
Vision Accelerator	7-way VLIW Processor	7-way VLIW Processor
Camera Expansion Header	16x CSI-2 Lanes (40 Gbps in D-PHY V1.2 or 109 Gbps in CPHY v1.1) 8x SLVS-EC Lanes (up to 18.4 Gbps) Up to 16 Simultaneous Cameras	16x CSI-2 Lanes (40 Gbps in D-PHY V1.2 or 64 Gbps in CPHY v1.1) 8x SLVS-EC Lanes (up to 18.4 Gbps) Up to 16 Simultaneous Cameras
PCIe	5x PCIe Gen4 (16GT/s) Controllers 1x8, 1x4, 1x2, 2x1 PCIe Gen4, Root Port and Endpoint	5x PCIe Gen4 (16GT/s) Controllers 1x8, 1x4, 1x2, 2x1 PCIe Gen3
Storage	32 GB eMMC 5.1	32 GB eMMC 5.1
UPHY	3x USB 3.1 (10 Gb/s) (4x) USB 2.0 ports 1 x8 or 1 x4 or 1 x2 or 2 x1 PCIe (Gen4)	3x USB 3.1, 4x USB 2.0 1 x8 or 1 x4 or 1 x2 or 2 x1 PCIe (Gen3)
Connectivity	1 Gigabit Ethernet, MAC, Reduced Gigabit Media Independent (RGMII) Interface	1 Gigabit Ethernet, MAC, Reduced Gigabit Media Independent (RGMII) Interface
Miscellaneous I/O's	UFS, I2S, i2c, SPI, CAN, GPIOs, UART, SD	UFS, I2S, i2c, SPI, CAN, GPIOs, UART, SD
Mechanical, Electrical, and Environmental Properties		
Form-Factor	H 3.93” x W 3.42” (100 x 87 mm; 16 mm Z-height)	
Weight	280 Grams (9.87 Ounces) +/- 10 grams with Packaging including Thermal Transfer Plate (TTP)	
Connector	699-Pin Board-to-Board Connector	
Cooling Solution	Integrated Thermal Transfer Plate (TTP) with Heat Pipe	
Power Input Range	9.0-20VDC	
Operating Temperature Range	25°C to 80°C	

3. FUNCTIONAL OVERVIEW

The following section provides functional details of the key sub-systems implemented on the baseboard.

3.1 Processor Modules

The baseboard currently supports the Jetson™ Series AGX Xavier Modules.

Both series, the AGX Xavier and Xavier 8 GB Modules integrate 512-core NVIDIA Volta GPU with Tensor Cores, and offer 16 GB of 256-bit LPDDR4x memory with 137 GB/s of bandwidth at 2133 MHz bus speeds that enable AI-powered platform tools to process high resolution computing tasks at 20 to 32 Tera Operations Per Second (TOPS) respectively.

The modules encapsulate a high-density 699-pin board-to-board connector for breaking out high-speed I/O signals to carrier board systems This enables seamless integration of applications and devices across a wide range of products and form-factors.

3.2 Power Supply Specifications

Elton baseboard is powered by a wide input voltage range of +9V to +20V.

Alternatively, the baseboard can be powered from a +12V input source on the PCIe/104 or PCI-04 power supply board by mounting the Jumper at location 5 on **JP3**. This disables the 5V and 3.3V power feed from the Elton baseboard to the PCIe/104 or PCI-104 Cards.

NOTE: The 12V pins on the PCI-104 connector are powered by the main input voltage. To meet the PCI-104 module I/O card requirements of 12V, the main input voltage supply unit must operate at +12V.

Power supply voltages for the baseboard are derived from the +(9V-20V) input source. The power supply unit must meet standards that support the highest bandwidth of on-board memory with additional reserves to support the add-on features listed in the table below.

Power Requirements for Supplementary Features

Feature	*12V*	*5V*	*3.3V*
AGX Xavier Series Module	2.5A		
PCI-104 and OneBank™ PCIe/104 Modules	1.0A	2A	2A
LCD Power	1.1A	1.4A	0.7A
PCIe MiniCard Socket			2A
M.2 SSD			0.5A
USB 2.0/3.1 (0.5A per USB 2.0 Port and 1A per USB 3.1 Port)		3A	
Camera Circuit		0.2A	0.4A
Second Ethernet Circuit			0.3A
Miscellaneous			1A

3.3 Backup Battery

The baseboard contains an on-board RTC (Real-Time Clock) battery holder which accommodates a BR-2032/BN coin cell. The default board configuration includes an installed coin cell. A 2 x1 input connector is provided to enable the use of an external battery for rugged applications.

3.4 Ethernet Ports

The baseboard is equipped with two Gigabit Ethernet ports.

1. A 10/100/1000 Ethernet port is derived from the Intel WGI210IT PCIe Ethernet controller which is accessed via x1 PCIe Lane routed from the module.
2. A 10/100/1000 Ethernet port is derived from the RGMII (Reduced Gigabit Media-Independent Interface) output of the module connected to the on-board KSZ9031 PHY from Microchip.

Each Port is equipped with on-board magnetics and 2x5 headers that are compatible with Diamond Systems standard Ethernet cables.

On-board LEDs are available to indicate the Link, Activity, and Speed status associated with each port. The LEDs are located along the board edge near the Ethernet connectors.

NOTE: The Ethernet port connectors do not provide access to the LED signals. Refer to Section: 3.18 LED Indicators for more details.

3.5 Display Controller

The baseboard supports HDMI 2.0 a/b Video Output. The HDMI port is routed from the AGX Xavier Series Module and is implemented through a 2x10 header.

Dual-channel LVDS interface functionality is obtained by connecting the Embedded DisplayPort™ (eDP) to a LVDS device such as the NXP PTN3460 bridge IC, to enable a dual-channel LVDS-LCD output.

The LCD Backlight control is implemented by a Pulse-Width Modulation (PWM) circuit which is located on a separate latching connector.

To implement a dual-channel on the LVDS-LCD output, the NXP PTN3460 bridge IC must be programmed to enable processes from the incoming DisplayPort (DP) stream, perform DP to LVDS protocol conversion between the Embedded DisplayPort (eDP) source and LVDS display panel. Refer to Section: Addendum for programming instructions.

3.6 Camera Serial Interface (CSI)

The AGX Xavier Series Module support four MIPI (Mobile Industry Processor Interface) CSI x4 bricks, enabling a wide array of device types and combinations to be implemented. Up to four 4-lane, six 2-lane, or six 1-lane configurations or combinations of camera streams are available. Each lane supports up to 16 Virtual Channels (VC). Each data channel has a peak bandwidth of up to 2.5 Gbps.

Similar to the Xavier Developer Kit Carrier Board, the baseboard supports four MIPI CSI x4 camera interfaces through a 120-pin daughterboard connector.

Add-on camera boards from Leopard Imaging/e-con Systems can be plugged into the daughterboard connector to support the four 4-lane or six 2-lane cameras. Alternatively, clients can customize a daughterboard to suit their requirements.

The daughterboard connector also supports i2c and control signals which enable users to directly interface the camera to the baseboard.

Refer to Section 17.2: Camera Installation Procedures of the Addendum for installation and operation procedures.

3.7 Audio Interface

The Audio Chip, Part Number SGTL5000 provides audio support on the baseboard. Audio I/O signals are generated through a 2mm header and include the following features:

- Stereo Line-Out
- Mic-In

The AGX Xavier Series Module implements a High Definition Audio (HDA) controller. The controller provides a multi-channel audio path to the HDMI (High-Definition Multimedia Interface) interface. The HDA Block provides an HDA-compliant serial interface to an audio codec. Multiple input and output streams are supported.

3.8 Serial Ports

Four serial ports are available on the baseboard 2x5 Header which are routed from the AGX Xavier Series Module through the programmable SP336 serial transceivers and implement selected RS232/422/485 protocols via GPIOs.

- All four serial ports are configured with the option to select RS232/422/485 protocol via GPIOs on the SP336 transceiver and are accessible through 2 nos. on the 2x5 header.
- Protocol selection is performed in a pairwise format such as Port 1-2 and Port 3-4.

An on-board Jumper option is provided to terminate RS422 and RS485 protocol transmission lines at 120 Ohm.

NOTE: By default, the Elton baseboard does not feature a Debug Serial Console Port but provides the ability to set up a Debug Serial Console by mounting the Jumper at location 6 on **JP3**. This will initiate the Serial Console configuration via serial port 1.

The serial port assignments on the baseboard are specified in the table below.

Port	*Connector*	*Assignment*
Port1	**J22**	ttyTHS0
Port2	**J22**	ttyTHS1
Port3	**J23**	ttyTHS4
Port4	**J23**	ttyTHS6

Refer to Section 17.3: Serial Multiprotocol Configurations of the Addendum for Multiprotocol Transceiver configuration modes.

3.9 PCIe/USB 3.1/UFS Link Routing Controllers

PCIe Controller

The AGX Xavier Series Module integrates a PCIe 4.0 compliant Root Port controller based on the Synopsys DesignWare PCIe Dual-Mode Controller that supports Gen1, Gen2, Gen3, and Gen4 link speeds up to 16 Gbps. The. Dual-Mode Controller supports PCIe endpoint mode operations and incorporates a Direct Memory Access (DMA) Engine to perform DMA data transfer.

NOTE: The Elton baseboard does not support PCIe Gen 4 interface.

USB 2.0/3.0/3.1 Controller

The AGX Xavier Series Module integrates both, an xHCI controller and a USB 3.0 device controller. The xHCI controller supports the xHCI Programming Model for scheduling transactions and interface managements as a Host. The series module natively supports USB 3.1, USB 2.0, and USB 1.1 transaction functionalities on its USB 3.1 and USB 2.0 interfaces.

The USB 3.0 device controller enables the AGX Xavier Series Module to be accessed from an external Host device. The controller supports USB 2.0 or USB 3.0 with up to 15 IN and 15 OUT Endpoints, which can be configured to support transfer types of different input devices such as a modem or a storage drive.

Both, the xHCI and USB 3.0 device controllers support USB Link Power Management (LPM) features: `Remote Wakeup`, `Wake On Connect`, `Wake On Disconnect`, and `Wake On Over Current`, in all power states, including `Deep Sleep` mode.

USB 3.1 ports support both, Gen 1-SuperSpeed and Gen 2-SuperSpeed at 10 Gbps transfer rates. USB 3.1 port 0 and port 3 share one 10 Gbps unit bandwidth, while USB 3.1 is allocated a separate 10 Gbps unit bandwidth. All USB 3.1 ports support hardware initiated U1 and U2 Link Power Management as well as software initiated U3 (suspend) Link Power Management.

Universal Flash Storage (UFS) Controller

The Universal Flash Storage controller in the AGX Xavier Series Module integrates the following blocks:

- A Universal Flash Storage Host Controller (UFSHC)
- A MIPI Unified Protocol (UniPro) Interface Controller
- Two MIPI M-PHY (MPHY) High-Speed Serial Interfaces

The UFS blocks can be operated in single (x1) or dual (x2) lane configurations to support operations at high-speed (HS)-G1, HS-G2, and HS-G3, at both, Rate A and Rate B speeds. MPHY modules drive the physical link and convert parallel data streams from the high-speed serializer into a high-speed differential or low-speed Pulse-Width Modulation (PWM)-like transmissions.

The PCIe, USB 3.1, and UFS Transport Protocol Mapping on the AGX Xavier Series Module are specified in the table below.

Signal/Pin Name	***Mapping***
UPHY0 (x1 PCIe)	1 to 5 Port PCIe Switch
UPHY1 (USB 3.1)	USB 3.1 Header
UPHY [5:2] (x4 PCIe)	M.2 PCIe
UPHY6 (USB 3.1)	USB 3.1 Header
UPHY7 (x1 PCIe)	I210 Ethernet Controller
UPHY8 (x1 PCIe)	PCIe to PCI Bridges
UPHY10 (x1 PCIe)	UFS Card Socket
NVHS0_ [7:0]	PCIe/104 Bank 2 and 3

A 6-port PCIe Gen 2 switch with x1 lane upstream port to 5nos of x1 downstream ports are utilized for effective IO expansion functionalities.

The downstream port assignments on the switch are specified in the table below.

Switch	***Port***	***Assignment***
PCIe Switch	Port1	PCIe/104 Bank1 Port1
PCIe Switch	Port2	PCIe/104 Bank1 Port2
PCIe Switch	Port3	PCIe/104 Bank1 Port3
PCIe Switch	Port4	PCIe/104 Bank1 Port4
PCIe Switch	Port5	Mini PCIe Card

3.10 PCIe MiniCard Socket

The baseboard is equipped with one Mini PCIe Socket that supports full-size modules.

Two threaded spacers are mounted on the board for installing a full-size module. A USB 2.0 interface is provided for plugging-in additional cards for expansion and connectivity. The USB 2.0 port is shared between the 2x5 Header in the Skywire™ 4G LTE Module –which is the default setting, and the PCIe MiniCard socket. This setting can be switched using the Jumper setting options.

3.11 PCI-104 and OneBank PCIe/104 Expansion Interface

Elton baseboard implements the PCI/104 Express (PCIe/104) interface functionalities through the PCI-104 connector and the 3-Bank PCIe/104 connector, respectively.

The PCI bus is realized by using a PCIe-PCI bridge such as the TI XIO2001. It supports both, 5V and 3.3V logic levels that are configurable with a Jumper.

4 x1 PCIe Gen 2 ports and 2 USB 2.0 ports are exposed via the OneBank connector. The x8 lane PCIe port from the AGX Xavier Series Module is connected directly to the 2nd and 3rd Banks on the PCIe/104 connector.

3.12 USB Ports

The baseboard provides 7x USB 2.0 ports and 2x USB 3.1 ports.

- 1x USB 2.0 port and 1x USB 3.1 ports are connected to 2x5 USB 3.0 header.
- 1x USB 2.0 port and 1x USB 3.1 ports are connected to 2x5 USB 3.0 header.
- 1x USB 2.0 port is muxed between the NimbeLink LTE module and MiniCard socket via Mux.

By default, it is connected to the NimbeLink LTE module and can be switched to the MiniCard socket using the Jumper option.

- 1x USB 2.0 port, routed from the AGX Xavier Series Module is connected to SMSC Part No. USB2514 USB 2.0 high-speed hub.
- 2x USB 2.0 ports from USB 2.0 Hub are connected to the 2x5 USB 2.0 header.
- 2x USB 2.0 ports from USB 2.0 Hub are connected to the PCIe/104 OneBank connector.

3.13 PCIe M.2 Socket

The baseboard provides a 2242 (22mm wide and 42mm long) form-factor M.2 PCIe SSD module socket with four PCIe lanes that are routed from the AGX Xavier Series Module.

3.14 UFS and Micro SD Socket

To enhance interoperability between devices, the baseboard supports a Universal Flash Storage (UFS) Card and MicroSD Card Combo socket with options to insert either or both cards.

3.15 Data Acquisition (DAQ) I/O Interface

The baseboard implements DAQ functionality via:

- Six Single-Ended (SE) Analog-Digital Converter (ADC) inputs or 3 Differential-Ended (DE) inputs
- Two Digital-to-Analog Converter (DAC) outputs
- 13 Digital I/Os through the SAM D51 microcontroller Series Part No. ATSAMD51J18A

All ADC, DAC, and Digital I/Os are available on the 2x13 header. The SAM microcontroller interfaces the AGX Xavier Series Module through a Serial Peripheral Interface (SPI) bus.

Refer to Section 14: Data Acquisition (DAQ) Subsystem for more information.

3.16 Controller Area Network (CAN) Interface

The AGX Xavier Series Module integrate two independent CAN ports/channels which support connectivity to two CAN networks. The CAN interfaces are routed to the baseboard via a 4-Pin Miniature 1.25mm Pitch latching connectors.

The TJA1050T CAN Transceiver interfaces between the CAN protocol controller and the physical bus. It enables high-speed automotive applications using baud rates from 60 Kbaud up to 1 Mbaud and provides differential transmission capabilities to the bus and differential receiver capabilities to the CAN protocol controller.

Refer to Section 17.4: CAN Controller Configuration of the Addendum on configuring the interface.

3.17 Utility Header Connector

A 2X3 Utility Header connector on the baseboard implements the Power button, Reset and Force Recovery signals through the on-board switches.

3.18 LED Indicators

The baseboard hosts the LED Indicators. The on-board LED Indicator panel is located to the left at the baseboard edge. The LEDs are displayed on a silkscreen panel with a description of their function and status as listed in the table below.

Led Indicators	***Description***
Power IN	Green LED indicates Power IN
Power ON	Green LED indicates Power ON
Host	Green LED indicates a Successful System Boot
User	Green LED indicates DAQ Controller Chip is ON
LED1	LED for Ethernet 2. Refer to Table below for Mode Indication
LED2	LED for Ethernet 2. Refer to Table below for Mode Indication
1G	1 Gbps Link indicator for Ethernet 1
100	100 Mbps Link indicator for Ethernet 1
ACT	Activity Link indicator for Ethernet 1

The following table defines LED-specific activity modes and the pin status associated with the modes.

Link Activity	***Pin State***		***LED Definition***	
	LED2	***LED1***	***LED2***	***LED1***
Link OFF	H	H	OFF	OFF
1000 Link/No Activity	L	H	ON	OFF
1000 Link/Activity (RX, TX)	Toggle	H	Blinking	OFF
100 Link/No Activity	H	L	OFF	ON
100 Link/Activity (RX, TX)	H	Toggle	OFF	Blinking
10 Link/No Activity	L	L	ON	ON
10 Link/Activity (RX, TX)	Toggle	Toggle	Blinking	Blinking

NOTE: According to the KSZ9031 Chip Errata, due to the high Tri-color Dual-LED mode pulse frequency, the blinking activity indication is not visible to the human eye.

4. FUNCTIONAL BLOCK DIAGRAM

4.1 Elton Baseboard Block Diagram

The following block diagram illustrates the key functional blocks of the Elton baseboard with integrated NVIDIA AGX Xavier Series Module and PCI/104 Express 3-Bank Expansion components.

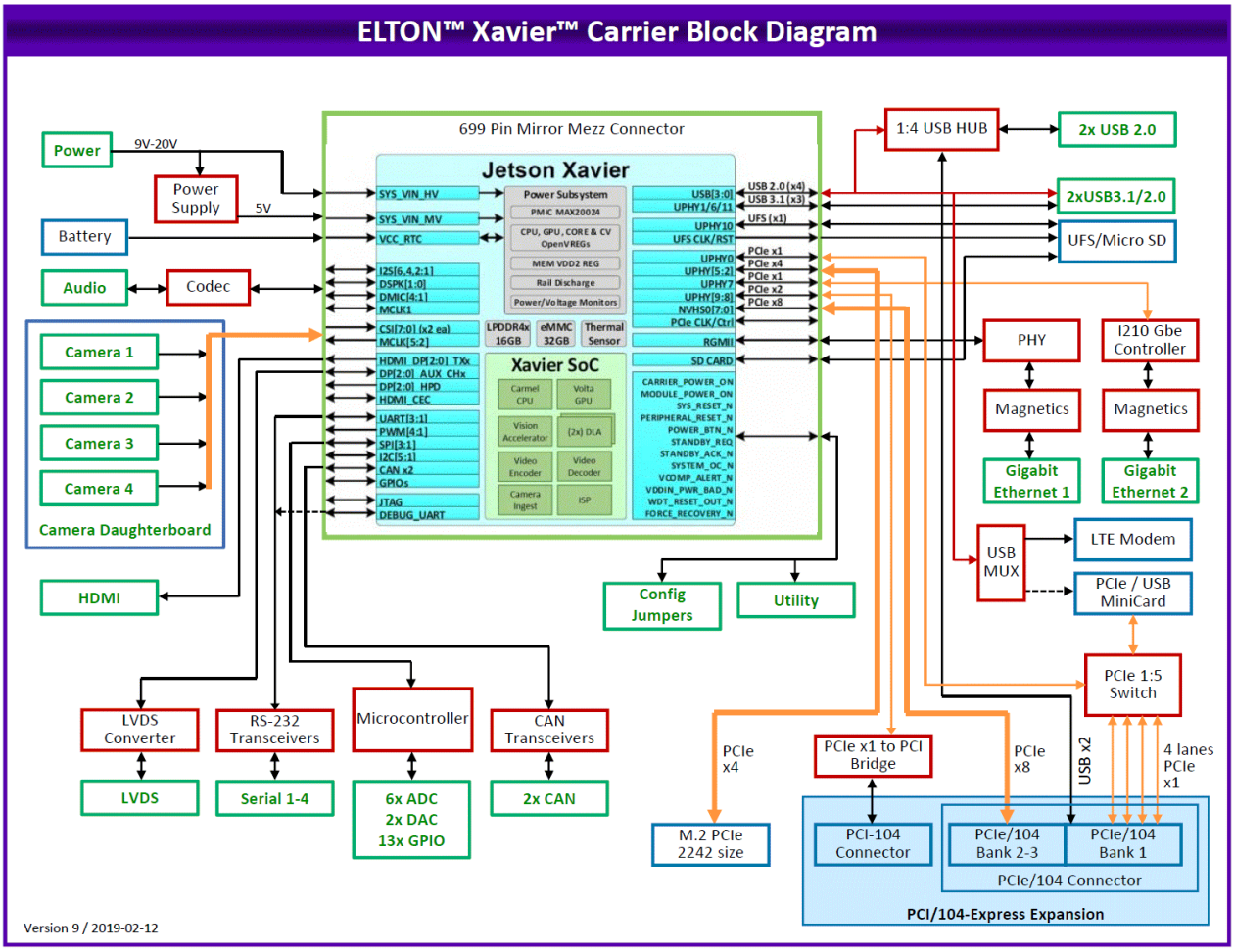


Figure 4.1-1: Baseboard Functional Block Diagram

4.2 AGX Xavier Series Module Block Diagram

The following block diagram illustrates a high-level view of the AGX Xavier Series components. The ports are broken out through the carrier board.

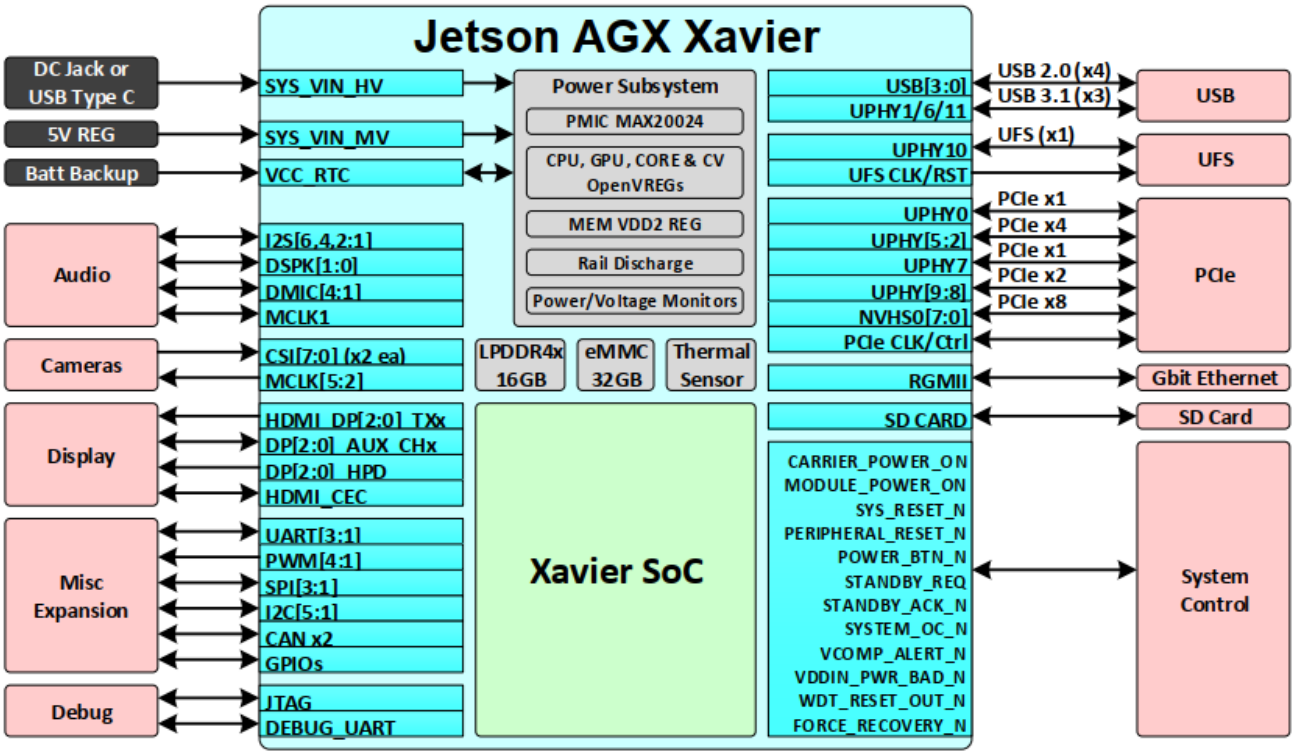


Figure 4.2-1: AGX Xavier Series Module Functional Block Diagram

5. MECHANICAL DRAWING

Figure 5-1 illustrates the mechanical top view of the Elton baseboard.

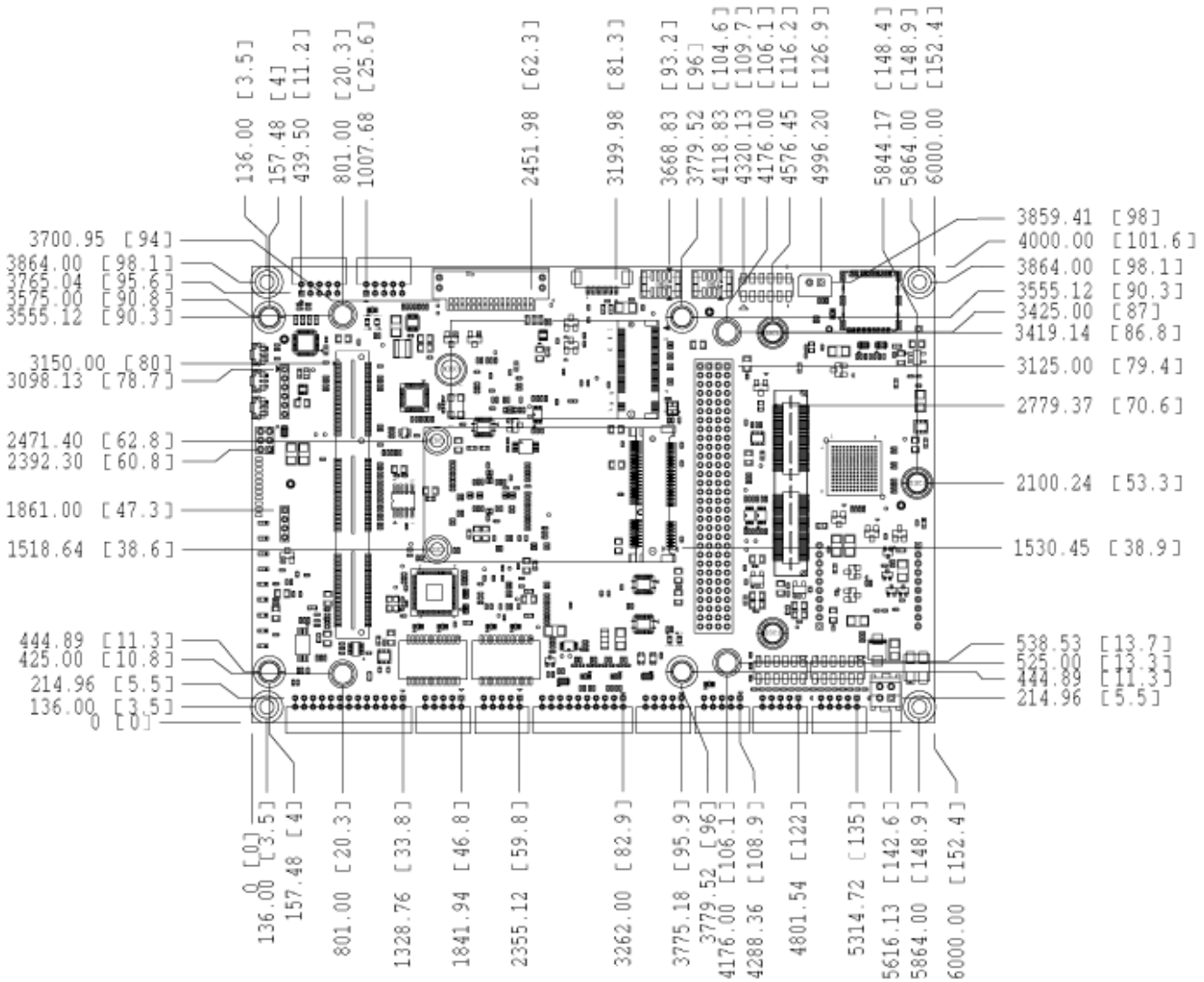


Figure 5-1: Elton Baseboard Mechanical Top View

6. CONNECTOR AND JUMPER LOCATION

Figure 6-1 displays the top and bottom layout views of the Elton baseboard. A description of the Jumpers and Connectors is tabulated below.

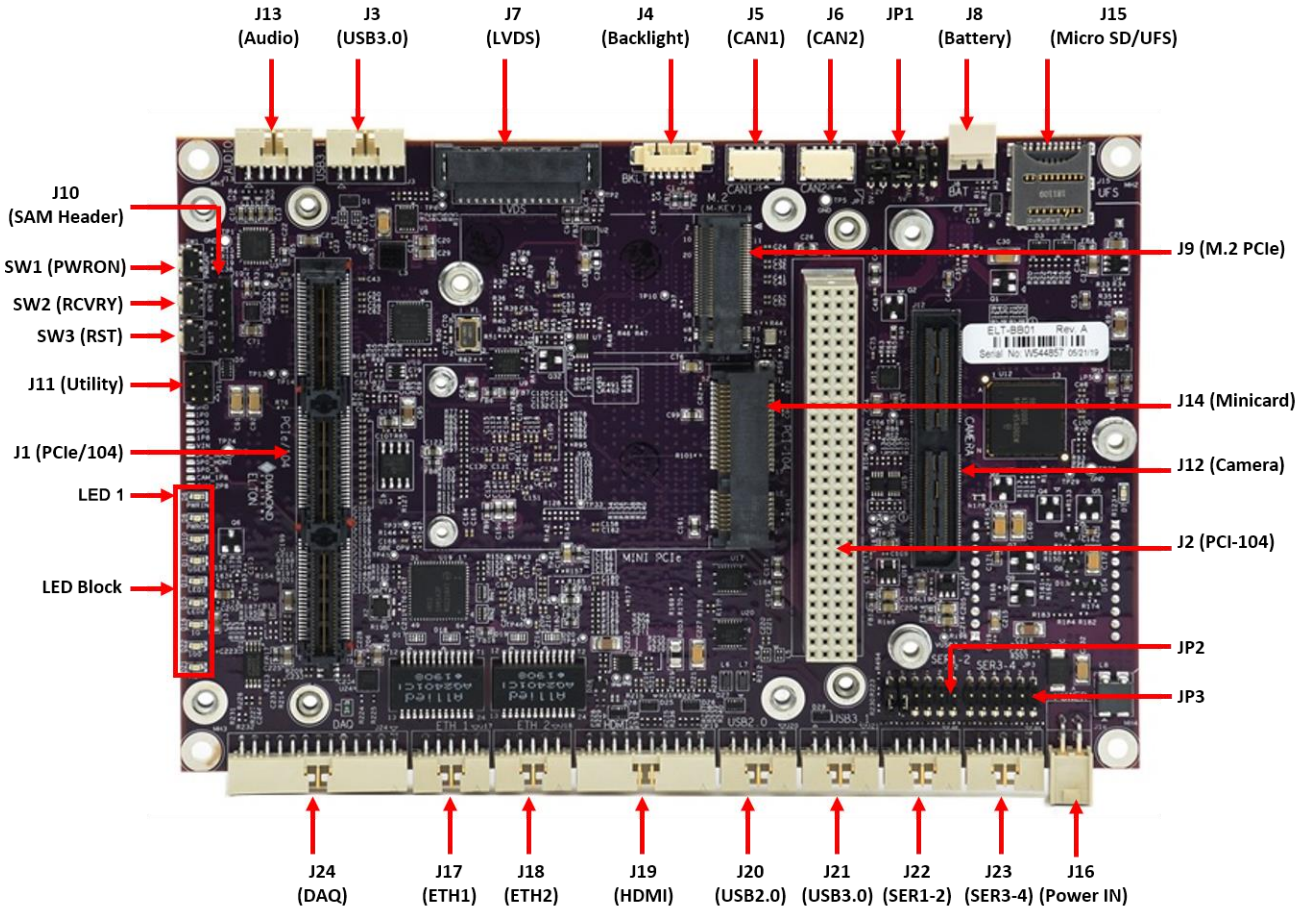


Figure 6-1: Baseboard Jumper and Connector Layout Top View

Figure 6-2 displays the bottom layout view of the Elton baseboard. A description of the Jumpers and Connectors is tabulated below.

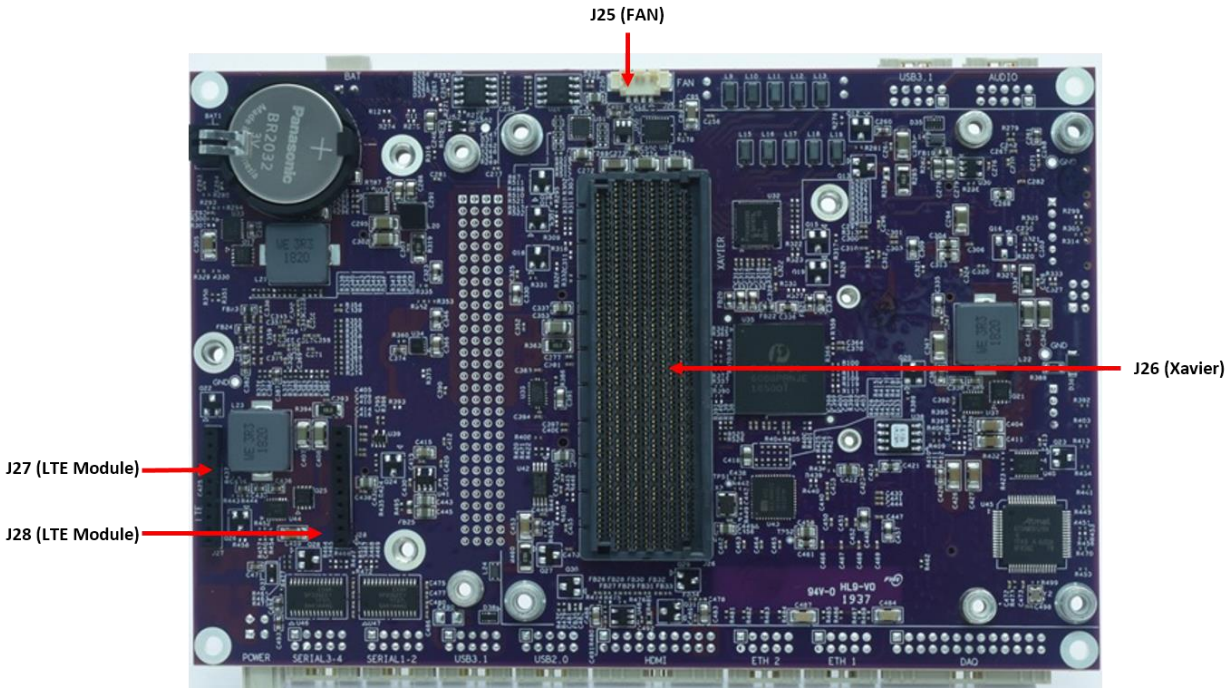


Figure 6-2: Baseboard Jumper and Connector Layout Bottom View

7. I/O CONNECTORS, JUMPERS AND LED SPECIFICATIONS

The following table delineates the I/O connectors, Jumpers, and LED Block functions, marked in Figure 6-1. and Figure 6-2.

Connector	*Function*
J1	PCIe/104
J2	PCI-104
J3	USB 3.1
J4	Backlight
J5	CAN1
J6	CAN2
J7	LVDS
J8	Battery
J9	M.2 KEY PCIe
J10	Programming Header
J11	Utility
J12	Camera
J13	Audio Codec
J14	Mini PCIe Card
J15	UFS Card
J16	Power IN
J17	ETH1
J18	ETH2
J19	HDMI
J20	USB 2.0
J21	USB 3.1
J22	Serial Ports 1-2
J23	Serial Ports 3-4
J24	DAQ
J25 (Bottom)	FAN
J26 (Bottom)	Xavier Module
J27 (Bottom)	LTE Module
J28 (Bottom)	LTE Module

Jumper	*Function*
JP1	LVDS_BKLT, LVDS_VDD, VIO_PCI
JP2	Serial Termination, USB Host, LTE USB Selection
JP3	Serial Termination, PCI Power Disable
LED Block	
1st LED: Marked in Figure 6-1	Power IN
2nd LED	Power ON
3rd LED	HOST LED
4th LED	SAM User LED
5th LED	LED1 for ETH2
6th LED	LED2 for ETH2
7th LED	1 Gbps link for ETH1
8th LED	100 Mbps link for ETH1
9th LED	Gbe ACT for ETH1

8. CONNECTOR PINOUT SPECIFICATIONS

8.1 Power IN Connector: J16

The Power-IN connector supplies power using an input voltage range from +9V to +20V.

NOTE: The AGX Xavier Series Module is not hot-pluggable. Before installing or removing the module, the main power supply pins must be disconnected and the recommended wait-time of 1-minute must be allowed for the various power rails to fully discharge.

The pinouts for the Power-IN connector are specified below.

VIN	**1**	**2**	GND
VIN	**3**	**4**	GND

Connector Type: 2x2 Samtec IPL1

Mating Cable Part Number: 6981507

8.2 RTC Battery Connector: J8

The RTC (Real Time Clock) battery provides power and maintains the internal real-time clock and calendar functions in the system.

The pinouts for the RTC Battery connector are specified below.

RTC_BATT	**1**
GND	**2**

Connector Type: 2x1 Header

Mating Cable Part Number: 6980524

8.3 Ethernet Connectors: J17, J18

The baseboard hosts two identical on-board connectors for the 10/100/1000 BASE T Ethernet.

The pinouts for the connectors are specified below.

ETH CH. Gnd	**A01**	**B01**	**Key**
DA+	**A02**	**B02**	DA-
DB+	**A03**	**B03**	DB-
DC+	**A04**	**B04**	DC-
DD+	**A05**	**B05**	DD-

Connector Type: 2mm Dual-Row Right Angle Pin Header

Mating Cable Part Number for Latching Connector: 6980604

Mating Cable Part Number for Pin Header: 6981080

8.4 Audio Signal Connector: J13

The audio signal interface implements audio-port switching functionality with digital microphone and speaker outputs.

The audio signals are terminated at the 2x5 header with the following pinouts.

NOTE: The Line-In feature is not supported by the Elton BSP (Board Support Package).

LineOut-L	**A01**	**B01**	LineOut-R
GND_Audio	**A02**	**B02**	GND_Audio
LineIn-L	**A03**	**B03**	LineIn-R
GND_Audio	**A04**	**B04**	GND_Audio
NC	**A05**	**B05**	MIC_IN

Connector Type: 2mm Dual-Row Right Angle Pin Header

Mating Cable Part Number for Latching Connector: 6980608

Mating Cable Part Number for Pin Header: 6981076

8.5 HDMI Connector: J19

The baseboard integrates a High Definition Multimedia Interface (HDMI) V2.0 interface The HDMI signals are terminated at the 2x10 header with the following pinouts.

The connector shell is tied to the Chassis Ground.

Data 2+	**A01**	**B01**	Ground
Data 2-	**A02**	**B02**	Data 1+
Ground	**A03**	**B03**	Data 1-
Data 0+	**A04**	**B04**	Ground
Data 0-	**A05**	**B05**	Clock+
Ground	**A06**	**B06**	Clock-
CEC	**A07**	**B07**	Reserved
DDC Clock	**A08**	**B08**	DDC Data
Ground	**A09**	**B09**	+5V
Hot Plug Detect	**A10**	**B10**	Chassis Ground

Connector Type: 2mm Dual-Row Right Angle Pin Header

Mating Cable Part Number for Latching Connector: 6980605

Mating Cable Part Number for Pin Header: 6980522

8.6 LVDS LCD Connector: J7

The Low-Voltage Differential Signaling (LVDS) LCD connector interface defines the physical layer parameters for differential, serial communication protocols and is used in conjunction with a data link layer.

It operates on low power and performs at high speeds.

The pinouts for the LVDS-LCD connector are specified below.

VDD 5V/3.3V	**1**	**2**	VDD 5V/3.3V
VDD 5V/3.3V	**3**	**4**	VDD 5V/3.3V
CLK+ Odd	**5**	**6**	CLK+ Even
CLK- Odd	**7**	**8**	CLK-Even
Ground	**9**	**10**	Ground
D0+ Odd	**11**	**12**	D0+ Even
D0- Odd	**13**	**14**	D0- Even
D1+ Odd	**15**	**16**	D1+ Even
D1- Odd	**17**	**18**	D1- Even
D2+ Odd	**19**	**20**	D2+ Even
D2- Odd	**21**	**22**	D2- Even
D3+ Odd	**23**	**24**	D3+ Even
D3- Odd	**25**	**26**	D3- Even
Ground	**27**	**28**	Ground
DDC CLK	**29**	**30**	DDC DATA

Connector Number/Type: TFM-115-02-L-DH; Side Entry; Type Pin Header

Mating Cable Part Number: Part Number is specific to the LCD Model in use.

8.7 LCD Backlight Connector: J4

The LCD backlight and the display data are powered by separate connectors. The pinouts for the LCD backlight connector are specified below.

1	Power, +5V/+12V, Jumper selectable
2	Power, +5V/+12V, Jumper selectable
3	Ground
4	Ground
5	Backlight Enable (GPIO output), 0 = off, open circuit = on
6	Brightness control

Connector Number/Type: JS-1147H-06; Right Angle, Type Friction Lock Pin Header

Mating Cable Part Number: Part Number is specific to the specified LCD Model in use.

8.8 USB 2.0 Port Connector: J20

The baseboard hosts two USB 2.0 ports The USB 2.0 interface connector features data and power pins on a pin header. The shield pin is tied to the Chassis Ground.

The pinouts for the USB 2.0 connector are specified below.

Key	A01	B01	Shield
USB1 Pwr-	A02	B02	USB0 Pwr-
USB1 Data+	A03	B03	USB0 Data+
USB1 Data-	A04	B04	USB0 Data-
USB1 Pwr+	A05	B05	USB0 Pwr+

Connector Type: 2mm Dual-Row Right Angle Pin Header

Mating Cable Part Number for Latching Connector: 6980602

Mating Cable Part Number for Pin Header: 6981082

8.9 PCIe/104 Connector: J1

The PCIe/104 connector is implemented to facilitate I/O expansion modules to plug into AGX Xavier Series Module baseboards.

Four x1 PCIe lanes and two USB 2.0 ports are connected to the OneBank PCIe/104 connector.

One number of x8 lane PCIe from the AGX Xavier Series Module is connected to the 2nd and 3rd Bank of the PCIe/104 connector.

The signal assignments for Banks 1 and 2 are depicted below.

Top View Signal Assignment				
1	USB_OC#		PE_RST#	2
3	3.3V		3.3V	4
5	USB_1p		USB_0p	6
7	USB_1n		USB_0n	8
9	GND		GND	10
11	PEx1_1Tp		PEx1_0Tp	12
13	PEx1_1Tn		PEx1_0Tn	14
15	GND		GND	16
17	PEx1_2Tp		PEx1_3Tp	18
19	PEx1_2Tn		PEx1_3Tn	20
21	GND		GND	22
23	PEx1_1Rp	+5 Volts	PEx1_0Rp	24
25	PEx1_1Rn		PEx1_0Rn	26
27	GND		GND	28
29	PEx1_2Rp		PEx1_3Rp	30
31	PEx1_2Rn		PEx1_3Rn	32
33	GND		GND	34
35	PEx1_1Clkp		PEx1_0Clkp	36
37	PEx1_1Clkn		PEx1_0Clkn	38
39	+5V_SB		+5V_SB	40
41	PEx1_2Clkp		PEx1_3Clkp	42
43	PEx1_2Clkn		PEx1_3Clkn	44
45	DIR		PWRGOOD	46
47	SMB_DAT		PEx16_Clkp	48
49	SMB_CLK		PEx16_Clkn	50
51			PSON#	52

Bank 1

Figure 8.9-1:Signal Assignment on Bank 1

53	STK0 / WAKE#			54
55	GND		GND	56
57			PEx16_0T(0)p	58
59			PEx16_0T(0)n	60
61	GND		GND	62
63			PEx16_0T(1)p	64
65			PEx16_0T(1)n	66
67	GND		GND	68
69			PEx16_0T(2)p	70
71			PEx16_0T(2)n	72
73	GND		GND	74
75			PEx16_0T(3)p	76
77			PEx16_0T(3)n	78
79	GND	+5 Volts	GND	80
81			PEx16_0T(4)p	82
83			PEx16_0T(4)n	84
85	GND		GND	86
87			PEx16_0T(5)p	88
89			PEx16_0T(5)n	90
91	GND		GND	92
93			PEx16_0T(6)p	94
95			PEx16_0T(6)n	96
97	GND		GND	98
99			PEx16_0T(7)p	100
101			PEx16_0T(7)n	102
103	GND		GND	104

Toward center of board

Bank 2

Figure 8.9-2: Signal Assignment on Bank 2

8.10 PCI-104 Connector: J2

The baseboard contains a non-stack-through/short pin PCI-104 connector located on top of the board in the standard position, as specified in the PC/104-Plus Specifications.

The **J3** connector pinouts are specified below.

		J3		
Pin	***A***	***B***	***C***	***D***
1	GND/5.0V KEY[2]	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY[2]

8.11 Camera Expansion Connector: J12

The AGX Xavier Series Module embeds a 2x60 expansion socket header for camera installation. The interface includes options for multiple cameras and audio signals.

The 4x4 CSI lanes from the AGX Xavier Series Module terminate at the 60x2 header.

The pinouts for the connector are specified below.

CSI_0_D0_P	1	2	CSI_1_D0_P
CSI_0_D0_N	3	4	CSI_1_D0_N
GND	5	6	GND
CSI_0_CLK_P	7	8	CSI_1_CLK_P
CSI_0_CLK_N	9	10	CSI_1_CLK_N
GND	11	12	GND
CSI_0_D1_P	13	14	CSI_1_D1_P
CSI_0_D1_N	15	16	CSI_1_D1_N
GND	17	18	GND
CSI_2_D0_P	19	20	CSI_3_D0_P
CSI_2_D0_N	21	22	CSI_3_D0_N
GND	23	24	GND
CSI_2_CLK_P	25	26	CSI_3_CLK_P
CSI_2_CLK_N	27	28	CSI_3_CLK_N
GND	29	30	GND
CSI_2_D1_P	31	32	CSI_3_D1_P
CSI_2_D1_N	33	34	CSI_3_D1_N
GND	35	36	GND
CSI_4_D0_P	37	38	CSI_6_D0_P
CSI_4_D0_N	39	40	CSI_6_D0_N
GND	41	42	GND
CSI_4_CLK_P	43	44	CSI_6_CLK_P
CSI_4_CLK_N	45	46	CSI_6_CLK_N
GND	47	48	GND
CSI_4_D1_P	49	50	CSI_6_D1_P
CSI_4_D1_N	51	52	CSI_6_D1_N
GND	53	54	GND
DVDD_CAM_LV	55	56	DVDD_CAM_LV
DVDD_CAM_LV	57	58	DVDD_CAM_LV
CSI_5_D0_P	59	60	CSI_7_D0_P
CSI_5_D0_N	61	62	CSI_7_D0_N
GND	63	64	GND

CSI_5_CLK_P	65	66	CSI_7_CLK_P
CSI_5_CLK_N	67	68	CSI_7_CLK_N
GND	69	70	GND
CSI_5_D1_P	71	72	CSI_7_D1_P
CSI_5_D1_N	73	74	CSI_7_D1_N
I2C_GP3_CLK	75	76	SNN_CAM_76
I2C_GP3_DAT	77	78	SNN_CAM_HSYNC
GND	79	80	GND
AVDD_CAM_2V8	81	82	AVDD_CAM_2V8
AVDD_CAM_2V8	83	84	VDD_AF
CAM_AF_PWDN	85	86	SNN_CAM_VSYNC
I2C_GP2_CLK	87	88	CAM1_MCLK03
I2C_GP2_DAT	89	90	GPIO15_CAM1_PWDN
CAM0_MCLK02	91	92	GPIO16_CAM1_RST
CAM0_PWDN	93	94	CAM2_MCLK04
CAM0_RST_BUFFER	95	96	SNN_CAM2_PWDN
SNN_FLASH_EN	97	98	SNN_CAM2_RST
GND	99	100	GND
DVDD_CAM_IO	101	102	VDD_1V8
SNN_FLASH_MASK	103	104	SNN_TORCH_EN
I2C_GP4_CLK	105	106	SNN_FLASH_STROBE
I2C_GP4_DAT	107	108	VDD_3V3
VDD_IR	109	110	VDD_3V3
SNN_SPI_SCK	111	112	SNN_SPI_DIN
SNN_SPI_CS0	113	114	SNN_SPI_DOUT
GND	115	116	GND
CAM_INTR	117	118	VDD_3V3
GPIO25_VDD_SYS_EN	119	120	VDD_3V3
GND	121	122	GND
GND	123	124	GND
GND	125	126	GND
GND	127	128	GND

Connector Number: Samtec QSH-060-01-H-D-A-K-TR

Mating Connector Part Number: Samtec QTH-060-01-L-D-A

8.12 Serial Port Connectors: J22, J23

The Elton baseboard supports four serial ports available at two headers. Each connector supports two serial ports.

The pinouts specific to transceiver interfaces RS232/ RS422/ RS485 are specified below.

RS-232 Interface

TX1	**A01**	**B01**	RTS1
RX1	**A02**	**B02**	CTS1
GND	**A03**	**B03**	GND
TX2	**A04**	**B04**	RTS2
RX2	**A05**	**B05**	CTS2

RS-422 (SP336) Interface

TX1+	**A01**	**B01**	TX1
RX1 +	**A02**	**B02**	RX1
GND	**A03**	**B03**	GND
TX2+	**A04**	**B04**	TX2
RX2+	**A05**	**B05**	RX2

RS-485 (SP336) Interface

TX1/RX1+	**A01**	**B01**	TX1/RX1
NC	**A02**	**B02**	NC
GND	**A03**	**B03**	GND
TX2/RX2+	**A04**	**B04**	TX2/RX2
NC	**A05**	**B05**	NC

Connector Type: 2mm Dual-Row; Right Angle Pin Header

Mating Connector Part Number for Latching Connector: 6980601

Mating Cable Part Number for Pin Header: 6981075

8.13 USB 3.1 Port Connectors: J3, J21

Two USB 3.0/3.1 connectors are available on the baseboard. Both are routed from the AGX Xavier Series Module to the 2x5 Header. The shield pin is tied to the Chassis Ground.

The pinouts for the connector are specified below.

USB_SSRX0-	**A01**	**B01**	**Shield**
USB_SSRX0+	**A02**	**B02**	USB1 Pwr-
USB1 Pwr-	**A03**	**B03**	USB2.0 Data+
USB_SSTX0-	**A04**	**B04**	USB2.0 Data-
USB_SSTX0+	**A05**	**B05**	USB Pwr+

Connector Type: 2mm Dual-Row; Right Angle Pin Header

Mating Connector Part Number for Latching Connector: 6980603

Mating Cable Part Number for Pin Header: 6980530

8.14 PCIe MiniCard Connector: J14

The TX (Transmit) and RX (Receive) signals are transmitted by the host.

The TX signal channels on the socket and the RX signal channels on the AGX Xavier Series Module are bi-directional. The RX signal on the socket is driven by the TX signal on the installed module and vice versa. The Chip Select (CS) control feature is available to generate commands on the SPI bus.

The two mounting standoffs at the far end of the AGX Xavier Series Module installation site are not connected to Ground.

The pinouts are specified below.

	1	**2**	+3.3V
	3	**4**	Gnd
	5	**6**	+1.5V
Clkreq-	**7**	**8**	
Gnd	**9**	**10**	
PCIe 1 Clk-	**11**	**12**	
PCIe 1 Clk+	**13**	**14**	
Gnd	**15**	**16**	
	KEY		
	17	**18**	Gnd
	19	**20**	Disable-
Gnd	**21**	**22**	PCIe Reset-
PCIe 1 RX-	**23**	**24**	+3.3V
PCIe 1 RX+	**25**	**26**	Gnd

Gnd	**27**	**28**	+1.5V
Gnd	**29**	**30**	SMB Clk
PCIe 1 TX-	**31**	**32**	SMB Data
PCIe 1 TX+	**33**	**34**	Gnd
Gnd	**35**	**36**	
Gnd	**37**	**38**	
+3.3V	**39**	**40**	Gnd
+3.3V	**41**	**42**	WWAN LED-
Ground	**43**	**44**	WLAN LED-
	45	**46**	WPAN LED-
	47	**48**	+1.5V
Pull-up to +3.3V	**49**	**50**	Gnd
	51	**52**	+3.3V

Connector Part Number: MM60-52B1-E1-R650

8.15 M.2 PCIe SSD Socket (M-KEY) Connector: J9

The Elton baseboard is equipped with an M-keyed connector.

An M.2 SSD is "keyed" to prevent the insertion of a card connector to an incompatible socket on the host. There are three keys that are commonly used: B, M, and B+M with the key type typically labeled on or near the edge of the gold-plated fingers on the connector of the SSD.

One mounting standoff at the far end of the module installation site is not connected to Ground. The pinouts for the connector are specified below.

GND	**1**	**2**	3.3V
GND	**3**	**4**	3.3V
PETn3	**5**	**6**	N/C
PETp3	**7**	**8**	N/C
GND	**9**	**10**	LED1#
PERn3	**11**	**12**	3.3V
PERp3	**13**	**14**	3.3V
GND	**15**	**16**	3.3V
PETn2	**17**	**18**	3.3V
PETp2	**19**	**20**	N/C
GND	**21**	**22**	N/C
PERn2	**23**	**24**	N/C
PERp2	**25**	**26**	N/C
GND	**27**	**28**	N/C
PETn1	**29**	**30**	N/C
PETp1	**31**	**32**	N/C
GND	**33**	**34**	N/C
PERn1	**35**	**36**	N/C
PERp1	**37**	**38**	N/C
GND	**39**	**40**	N/C
PETn0	**41**	**42**	N/C
PETp0	**43**	**44**	N/C
GND	**45**	**46**	N/C
PERn0	**47**	**48**	N/C
PERp0	**49**	**50**	PERST#
GND	**51**	**52**	CLKREQ#
REFCLKN	**53**	**54**	PEWake#
REFCLKP	**55**	**56**	N/C
GND	**57**	**58**	N/C
	KEY		
N/C	**67**	**68**	SUSCLK
PEDET	**69**	**70**	3.3V
GND	**71**	**72**	3.3V
GND	**73**	**74**	3.3V
GND	**75**		

Connector Part Number: 6980603

8.16 Data Acquisition (DAQ) Connector: J24

The baseboard implements a multifunction Digital I/O circuit that integrates analog input and output, digital input and output, and counter/timer functionalities.

The pinouts for the connector specified below.

AIN0 / 0-	**A01**	**B01**	AIN1 / 0+
AIN2 / 1-	**A02**	**B02**	AIN3 / 1+
AIN4 / 2-	**A03**	**B03**	AIN5 / 2+
DAC0	**A04**	**B04**	DAC1
Aground	**A05**	**B05**	Aground
Dground	**A06**	**B06**	+3.3V Fused
DIO 0	**A07**	**B07**	DIO 1
DIO 2	**A08**	**B08**	DIO 3
DIO 4	**A09**	**B09**	DIO 5
DIO 6	**A10**	**B10**	DIO 7
DIO 8	**A11**	**B11**	DIO 9
DIO 10	**A12**	**B12**	DIO11
DIO 12 /RESET_IN	**A13**	**B13**	Dground

The following table provides the signal type and its definition.

Signal Name	***Definition***
AIN 5-0/AIN 2-0	Single / Differential Ended Analog Inputs at 3.3V Level
DAC 1-0	DAC Outputs at 3.3V Level
DIO 11-0	Digital I/O Port. Programmable Direction at 3.3V Level
DIO 12 /RESET_IN	Digital IO at 3.3V Level. Reset In Signal at 1.8V Level
Dground	Digital Ground
Aground	Analog Ground

Connector Type: Standard 2mm Dual-Row; Straight Pin Header

Mating Connector Part Number for Latching Connector: 6980606

Mating Cable Part Number for Pin Header: 6980516

8.17 Utility Connector: J11

The following table provides the pinouts for the power utility connector.

Force Recovery	**1**	**2**	Ground
Reset In	**3**	**4**	Ground
Power Button	**5**	**6**	Ground

Connector Type: Standard 2mm Dual-Row; Straight Pin Header

Cable Part Number: TBD

8.18 CAN Connectors: J5, J6

There are two identical on-board CAN interface connectors that are routed from the AGX Xavier Series Module. The pinouts are specified below.

Ground	**1**
CAN Low	**2**
CAN High	**3**
Ground	**4**

Connector Type: 1.25mm Single Row SMD RA

Cable Part Number: 6981182

8.19 UFS Interface Connector: J15

The AGX Xavier Series Module supports a x1 lane UFS interface.

The pinouts for the connector are specified below.

1	VSS
2	DIN_C
3	DIN_T
4	VSS
5	DOUT_C
6	DOUT_T
7	VSS
8	REFCLK
9	VCCQ2
10	GND
11	VSS
12	VCC
13	DATA1

14	DATA0
15	CLK
16	CMD
17	DATA3
18	DATA2
19	C_DETECT
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND

Connector Type: Standard UFS + Micro SD Connector

Manufacturer: Amphenol

9. I/O CONNECTOR LIST

The following table provides a summary of the I/O connectors on the Elton baseboard.

Function	*Manufacturer*	*Part No.*	*Description*	*DSC Mating Cable*
Power IN	Samtec	IPL1-102-01-D-RA-K	2x2 Box Header T/H Right Angle .1 Pitch	6981507
External Battery	Molex	22-035-5025	2 Pos. TH VERT RA HDR, 2.5 MM Shrouded	6980524
GbE Ethernet (x2)	FCI	98414-F06-10ULF	2x5, 2mm Pitch, TH Header RA	6980604
LVDS	Samtec	TFM-115-02-L-DH	2x 15, 1.25MM SMT, RA	NA
LCD Backlight	Chyao-Shiunn	JS-1147H-06	6 pos. 1.25mm Pitch, SMT, RA	NA
HDMI	FCI	98414-F06-20ULF	2x10, 2mm Pitch, TH Header RA	6980605
Camera (x4)	Samtec	QSH-060-01-H-D-A-K-TR	2x60 0.5mm Pitch	NA
Serial Ports (x4)	FCI	98414-F06-10ULF	2x5, 2mm Pitch, TH Header RA	6980601
Audio	FCI	98414-F06-10ULF	2x5, 2mm Pitch, TH Header RA	6980608
USB 3.1 (x2)	FCI	98414-F06-10ULF	2x5, 2mm Pitch, TH Header RA	6980603
USB 2.0	FCI	98414-F06-10ULF	2x5, 2mm Pitch, TH Header RA	6980602
CAN (x2)	JST	SM04B-GHS-TB	1x4, 1.25mm Pitch, SMT RA	6981182
DAQ	FCI	98414-F06-26ULF	2x13, 2mm Pitch, TH Header RA	6980606
Utility	PINREX	220-9203GB01	2x3, 2mm Pitch, TH Header	N/A
PCIe MiniCard	JAE	MM60-52B1-E1-R650	52-Pin MiniCard, Full Size, with PCB Mount Threaded Spacers	N/A
PCI-104	EPT	264-61303-02	30 x 4 pin 2mm Pitch with Solder Tails	N/A
PCIe 3 Bank	Samtec	ASP-142781-03s	156 Pos. Top Mount	N/A
M.2 SSD Socket	Amphenol	MDT320M03001	75-pin M.2 M Keyed Socket, 2242 with PCB Mount Threaded Spacer	N/A
UFS	Amphenol	1010170469#2A	CONN UFS and Micro SD Push-Pull	N/A
Module Connector	Molex	2034560003	699-Pin Board-to-Board Connector/B, 8mm	N/A

9.1 I/O Cables

CK-ELTON-01 Package

CK-ELTON-01 Non-Latching Cables are industry-standard cables that are required during installation. The following table provides Non-Latching Cable specifications included in the CK-ELTON-01 package.

Photo No	*Cable Part No.*	*Description*	*Elton Connector*
1	6981507	Power Cable	**J16**
2	6980524	External Battery	**J8**
3	6980601	Serial Ports	**J22**, **J23**
4	6980602	USB 2.0 TYPE A Panel Mount	**J20**
5	6980603	USB 3.0 TYPE A Panel Mount	**J3**, **J21**
6	6980604	RJ-45 Socket	**J17**, **J18**
7	6980605	HDMI Cable	**J19**
8	6980606	DAQ Cable	**J24**
9	6980608	Audio Cable	**J13**
10	6981182	CAN Bus 2.0 Cable	**J5**, **J6**

10. JETSON XAVIER B2B CONNECTOR INTERFACE

The following table figure depicts Jetson AGX Xavier Series Module Connector Pin Out Matrix Part 1: Columns A – F.

	A	B	C	D	E	F
01			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
02			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
03	PRSNT0	SYS_VIN_HV	GND	SYS_VIN_HV	GND	SYS_VIN_HV
04	SDCARD_D2	GND	RGMII_RD0	GND	I2S2_FS	GND
05	SDCARD_CMD	RGMII_TXC	RGMII_RXC	RGMII_RX_CTL	RGMII_RD3	I2S2_DOUT
06	UFS0_REF_CLK	SDCARD_CLK	UFS0_RST_N	SDCARD_D3	RGMII_SMA_MDC	I2S2_DIN
07	GPIO29	GND	I2S1_SDOUT	GND	RGMII_SMA_MDIO	GND
08	PEX_WAKE_N	GPIO11	PEX_L5_CLKREQ_N	I2S1_FS	SDCARD_D0	SDCARD_D1
09	GND	PEX_L1_RST_N	GND	PEX_L1_CLKREQ_N	GND	GPIO16
10	USB2_P	RSVD	USB1_N	PEX_L0_RST_N	GPIO12	GPIO15
11	USB2_N	GND	USB1_P	GND	PEX_L0_CLKREQ_N	GND
12	GND	UPHY_RX10_P	GND	UPHY_RX11_P	GND	USB0_P
13	GND	UPHY_RX10_N	GND	UPHY_RX11_N	GND	USB0_N
14	UPHY_RX8_N	GND	UPHY_RX9_N	GND	PEX_CLK0_N	GND
15	UPHY_RX8_P	GND	UPHY_RX9_P	GND	PEX_CLK0_P	GND
16	GND	UPHY_RX6_P	GND	UPHY_RX7_P	GND	PEX_CLK1_P
17	GND	UPHY_RX6_N	GND	UPHY_RX7_N	GND	PEX_CLK1_N
18	UPHY_RX4_P	GND	UPHY_RX5_N	GND	RSVD	GND
19	UPHY_RX4_N	GND	UPHY_RX5_P	GND	RSVD	GND
20	GND	UPHY_RX2_N	GND	UPHY_RX3_P	GND	PEX_CLK3_P
21	GND	UPHY_RX2_P	GND	UPHY_RX3_N	GND	PEX_CLK3_N
22	UPHY_RX0_P	GND	UPHY_RX1_N	GND	PEX_CLK4_N	GND
23	UPHY_RX0_N	GND	UPHY_RX1_P	GND	PEX_CLK4_P	GND
24	GND	NVHS0_SLVS_RX1_N	GND	NVHS0_SLVS_RX0_P	GND	PEX_CLK5_P
25	GND	NVHS0_SLVS_RX1_P	GND	NVHS0_SLVS_RX0_N	GND	PEX_CLK5_N
26	NVHS0_SLVS_RX3_P	GND	NVHS0_SLVS_RX2_N	GND	UPHY_REFCLK1_N	GND
27	NVHS0_SLVS_RX3_N	GND	NVHS0_SLVS_RX2_P	GND	UPHY_REFCLK1_P	GND
28	GND	NVHS0_SLVS_RX5_N	GND	NVHS0_SLVS_RX4_P	GND	RSVD
29	GND	NVHS0_SLVS_RX5_P	GND	NVHS0_SLVS_RX4_N	GND	RSVD
30	NVHS0_SLVS_RX7_P	GND	NVHS0_SLVS_RX6_N	GND	NVHS0_SLVS_REFCLK0_P	GND
31	NVHS0_SLVS_RX7_N	GND	NVHS0_SLVS_RX6_P	GND	NVHS0_SLVS_REFCLK0_N	GND
32	GND	RSVD	GND	RSVD	GND	RSVD
33	GND	RSVD	GND	RSVD	GND	RSVD
34	RSVD	GND	RSVD	GND	RSVD	GND
35	RSVD	GND	RSVD	GND	RSVD	GND
36	GND	RSVD	GND	RSVD	GND	RSVD
37	GND	RSVD	GND	RSVD	GND	RSVD
38	RSVD	GND	RSVD	GND	CSI0_D1_N	GND
39	RSVD	GND	RSVD	GND	CSI0_D1_P	GND
40	GND	MID4	GND	MID3	GND	MID2
41	CSI2_D0_P	GND	CSI2_D1_N	GND	CSI0_D0_N	GND
42	CSI2_D0_N	CSI2_CLK_N	CSI2_D1_P	CSI5_D0_P	CSI0_D0_P	CSI0_CLK_N
43	GND	CSI2_CLK_P	GND	CSI5_D0_N	GND	CSI0_CLK_P
44	CSI7_D0_P	GND	CSI5_CLK_P	GND	CSI3_D0_N	GND
45	CSI7_D0_N	CSI7_CLK_P	CSI5_CLK_N	CSI5_D1_N	CSI3_D0_P	CSI3_CLK_N
46	GND	CSI7_CLK_N	GND	CSI5_D1_P	GND	CSI3_CLK_P
47	HDMI_DP1_TX0_P	GND	CSI7_D1_P	GND	CSI4_D1_P	GND
48	HDMI_DP1_TX0_N	HDMI_DP1_TX1_N	CSI7_D1_N	HDMI_DP1_TX2_N	CSI4_D1_N	CSI4_CLK_P
49	GND	HDMI_DP1_TX1_P	GND	HDMI_DP1_TX2_P	GND	CSI4_CLK_N
50	HDMI_DP2_TX2_N	GND	HDMI_DP2_TX3_N	GND	HDMI_DP1_TX3_P	GND
51	HDMI_DP2_TX2_P	HDMI_DP2_TX1_P	HDMI_DP2_TX3_P	HDMI_DP2_TX0_P	HDMI_DP1_TX3_N	DP0_AUX_CH_N
52	GND	HDMI_DP2_TX1_N	GND	HDMI_DP2_TX0_N	GND	DP0_AUX_CH_P
53	I2C5_CLK	GND	I2C5_DAT	GND	I2C3_DAT	I2C3_CLK
54	GPIO17	WDT_RESET_OUT_N	GPIO33	GPIO03	FAN_TACH	GPIO22
55	GPIO34	GPIO30	GPIO18	SPI1_MOSI	SPI1_CS0_N	SPI3_CLK
56	SPI1_MISO	SPI1_CS1_N	UART2_RX	SPI3_MISO	SPI3_CS1_N	GPIO36
57	UART2_CTS	GND	SPI3_CS0_N	GND	GND	GND
58	GPIO20	GPIO21	UART2_TX	JTAG_TDO	JTAG_TMS	CAN0_DIN
59	GPIO05	GPIO04	I2S3_SCLK	CAN0_DOUT	GPIO06	GPIO07
60	JTAG_TCK	JTAG_TDI	I2S3_FS	SPI2_CS0_N	I2C4_DAT	SPI2_MOSI
61	SYSTEM_OC_N	CAN1_DIN	GPIO09	I2C4_CLK	SPI2_CLK	VCOMP_ALERT_N
62	GPIO10	GPIO08	GND	SPI2_MISO	GND	GND
63	GND	SYS_VIN_HV	SYS_VIN_HV	GND	SYS_VIN_HV	SYS_VIN_HV
64			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
65			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV

Legend: Ground | Power | Reserved–Must be left unconnected unless otherwise directed

The following table figure depicts Jetson AGX Xavier Series Module Connector Pin Out Matrix Part 2: Columns G – L.

	G	H	J	K	L
01	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
02	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
03	GND	SYS_VIN_HV	GND	SYS_VIN_HV	GND
04	I2S2_CLK	GND	GPIO01	GND	UART4_RTS
05	RGMII_TD1	ENET_RST_N	ENET_INT	I2C1_CLK	UART4_TX
06	RGMII_TD3	RGMII_RD2	RGMII_TD0	RGMII_RD1	GPIO02
07	GPIO13	GND	RGMII_TD2	RGMII_TX_CTL	GND
08	PEX_L4_CLKREQ_N	I2S1_SDIN	GND	GND	I2C1_DAT
09	GND	MCLK01	PEX_L4_RST_N	PEX_L3_RST_N	GPIO28
10	USB3_N	PEX_L5_RST_N	PEX_L3_CLKREQ_N	RSVD	FORCE_RECOVERY_N
11	USB3_P	GND	RSVD	GND	STANDBY_REQ_N
12	GND	UPHY_TX11_P	GND	UPHY_TX10_N	GND
13	GND	UPHY_TX11_N	GND	UPHY_TX10_P	GND
14	UPHY_TX9_N	GND	UPHY_TX8_P	GND	I2S1_CLK
15	UPHY_TX9_P	GND	UPHY_TX8_N	GND	GPIO14
16	GND	UPHY_TX7_P	GND	UPHY_TX6_N	GND
17	GND	UPHY_TX7_N	GND	UPHY_TX6_P	GND
18	UPHY_TX5_N	GND	UPHY_TX4_P	GND	RSVD
19	UPHY_TX5_P	GND	UPHY_TX4_N	GND	RSVD
20	GND	UPHY_TX3_P	GND	UPHY_TX2_N	GND
21	GND	UPHY_TX3_N	GND	UPHY_TX2_P	GND
22	UPHY_TX1_N	GND	UPHY_TX0_P	GND	SYS_VIN_MV
23	UPHY_TX1_P	GND	UPHY_TX0_N	GND	SYS_VIN_MV
24	GND	NVHS0_TX0_P	GND	NVHS0_TX1_N	GND
25	GND	NVHS0_TX0_N	GND	NVHS0_TX1_P	GND
26	NVHS0_TX2_N	GND	NVHS0_TX3_P	GND	SYS_VIN_MV
27	NVHS0_TX2_P	GND	NVHS0_TX3_N	GND	SYS_VIN_MV
28	GND	NVHS0_TX4_P	GND	NVHS0_TX5_N	GND
29	GND	NVHS0_TX4_N	GND	NVHS0_TX5_P	GND
30	NVHS0_TX6_N	GND	NVHS0_TX7_P	GND	SYS_VIN_MV
31	NVHS0_TX6_P	GND	NVHS0_TX7_N	GND	SYS_VIN_MV
32	GND	RSVD	GND	RSVD	GND
33	GND	RSVD	GND	RSVD	GND
34	RSVD	GND	RSVD	GND	SYS_VIN_MV
35	RSVD	GND	RSVD	GND	SYS_VIN_MV
36	GND	RSVD	GND	RSVD	GND
37	GND	RSVD	GND	RSVD	GND
38	RSVD	GND	RSVD	GND	SYS_VIN_MV
39	RSVD	GND	RSVD	GND	SYS_VIN_MV
40	GND	MID1	GND	MID0	GND
41	CSI1_D0_P	GND	CSI1_D1_P	GND	VM_EN1_N
42	CSI1_D0_N	CSI1_CLK_N	CSI1_D1_N	GND	VM_EN0_N
43	GND	CSI1_CLK_P	GND	CSI6_D0_N	GND
44	CSI3_D1_P	GND	CSI6_CLK_P	CSI6_D0_P	VM_I2C_SCK
45	CSI3_D1_N	CSI6_D1_N	CSI6_CLK_N	GND	VM_I2C_DAT
46	GND	CSI6_D1_P	GND	HDMI_DP0_TX3_P	GND
47	CSI4_D0_N	GND	HDMI_DP0_TX2_P	HDMI_DP0_TX3_N	VM_INT_N
48	CSI4_D0_P	HDMI_DP0_TX0_N	HDMI_DP0_TX2_N	GND	UART4_RX
49	GND	HDMI_DP0_TX0_P	GND	GPIO25	UART4_CTS
50	HDMI_DP0_TX1_N	GND	HDMI_CEC	DP2_HPD	GPIO35
51	HDMI_DP0_TX1_P	GPIO26	GPIO24	DP1_HPD	UART1_RTS
52	GND	GPIO27	DP1_AUX_CH_P	DP0_HPD	OVERTEMP_N
53	DP2_AUX_CH_P	MCLK03	DP1_AUX_CH_N	UART1_TX	VCC_RTC
54	DP2_AUX_CH_N	UART1_CTS	MCLK02	UART1_RX	MODULE_POWER_ON
55	GPIO23	MCLK04	GPIO32	GND	VDDIN_PWR_BAD_N
56	SPI3_MOSI	GND	GND	GPIO19	TEMP_ALERT_N
57	GND	UART5_CTS	SPI1_CLK	PWM01	MCLK05
58	UART2_RTS	UART5_RX	UART5_TX	UART5_RTS	PERIPHERAL_RESET_N
59	NC_03	NVJTAG_SEL	I2S3_DIN	I2S3_DOUT	SAFETY_PROCESSOR_GPIO
60	NVDBG_SEL	GPIO31	STANDBY_ACK_N	UART3_RX_DEBUG	SYS_RESET_N
61	JTAG_TRST_N	CAN1_DOUT	I2C2_CLK	I2C2_DAT	POWER_BTN_N
62	GND	UART3_TX_DEBUG	GND	FAN_PWM	CARRIER_POWER_ON
63	SYS_VIN_HV	GND	SYS_VIN_HV	GND	PRSNT1
64	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
65	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		

Legend	Ground	Power	Reserved – Must be left unconnected unless otherwise directed. See UART section for UART4_RX handling in the OEM PRODUCT DESIGN GUIDE: NVIDIA Jetson AGX Xavier Series

11. PC/104 EXPANSION SYSTEM

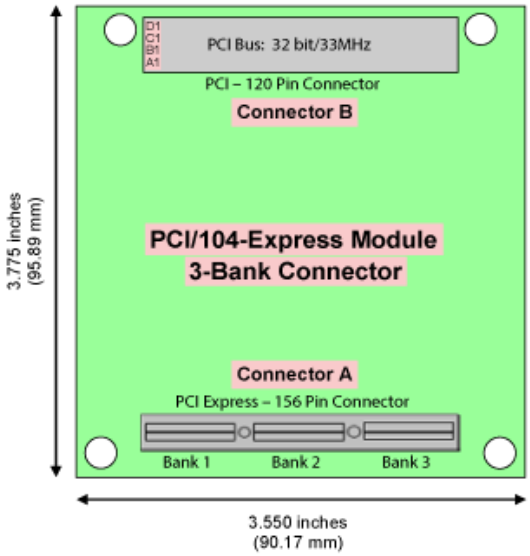
11.1 Overview

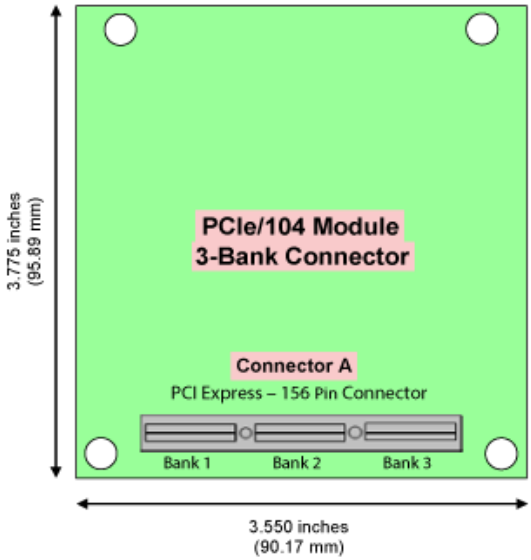
Elton baseboard embeds the PC/104 Expansion Module that integrates PCI and PCIe connectors in a compact-sized form-factor measuring approximately 3.6" x 3.8" (90mm x 96mm).

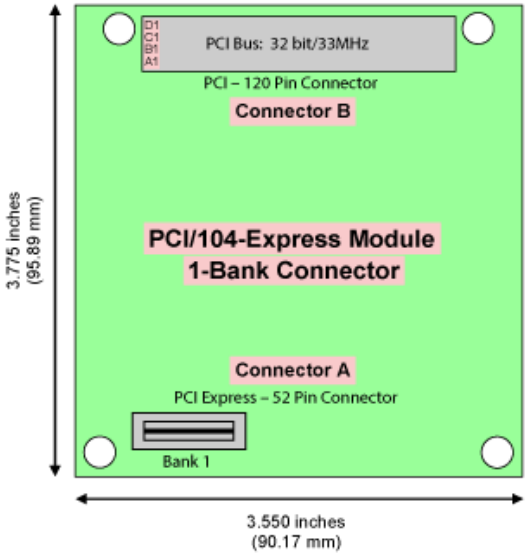
The PCI Express (Peripheral Component Interconnect Express/PCIe) architecture improvises on the conventional PCI bus configurations to deliver the next generation PC/104 high-speed serial bus expansion system, implemented by a pair of surface mount connectors in a slot-oriented platform that incorporates a non-conventional point-to-point interface technology, while still retaining compatibility within the conventional PCI framework.

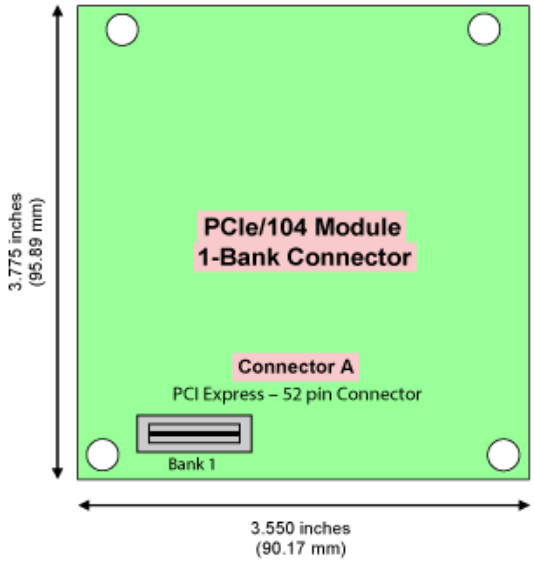
Designed for stackability and system expansion, the PC/104 Module with the OneBank implementation capabilities offers scalability, extensibility, and modularity, suitable for all environments, including Military, Transportation, Industrial and Aviation sectors.

The following figures present an overview of the PC/104 board layouts on 104 form factors with Express Connectors, Three Banks and OneBank respectively.









11.1 Functional Block Diagram

The following block diagram illustrates the functional blocks of the PC/104 Module interconnected with NVIDIA AGX Xavier Series Module, PCI/104 Express 3-Bank expansion components, and the expansion PCI bus connector.

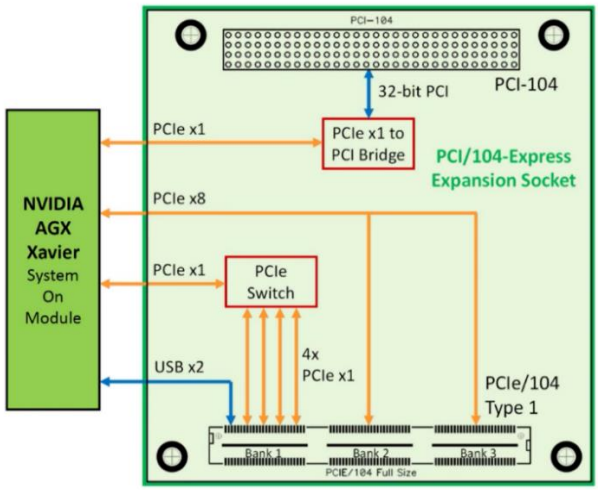


Figure 11.1-1: PC/104 Express Block Diagram

11.2 PC/104 Bus Framework

The PC/104 Consortium specifications framework encapsulate standards related to ISA, PCI, and PCI Express buses used in a PC.

PC/104 Bus

The PC/104 bus is derived from the ISA bus and includes all the signals found on the ISA bus, with additional Ground pins added to ensure bus integrity. Signal timing and voltage levels are identical to the ISA bus, with lower current requirements. The PC/104 specification defines two versions of the bus, 8-bit and 16-bit. The 8-bit version consists of 64 pins. The 16-bit version adds 40 additional pins. The term "PC/104" denotes the total number of 104 pins on the connector.

The pinouts for the PC/104 connector can be obtained from the PC/104 Signal Assignments site. The signals marked **J1**/**P1** are found only on the 8-bit version, while **J2**/**P2** are found on the 16-bit version.

PC/104 supports ISA only.

PC/104-Plus Bus

The PC/104-Plus standard adds additional support for the PCI bus, besides the PC/104 ISA bus. The PC/104-Plus module contains a PC/104 connector and an additional 120-pin connector for the PCI bus that is located on the opposite side of the board from the PC/104 connector.

The pinouts for the PCI connector can be obtained from the PCI-104 Bus Pinout site.

Boards equipped with PC/104-Plus accommodate both buses that interconnect with both ISA and PCI peripheral cards.

PC/104-Plus supports PCI and ISA only.

PCI-104 Bus

The PCI-104 form factor incorporates the PCI connector but not the PC/104 connector. It contains 120 pins. The PCI connector location and pinout is identical to PC/104-Plus and does not include the ISA bus.

PCI-104 and PC/104-Plus are compatible since they both utilize the PCI bus and also the same PCI Slot Number selection scheme, where each device must be assigned a unique slot number.

PCI-104 supports PCI only.

The following schematic represents the PC/104 120-pin expansion bus connector and dimensions.

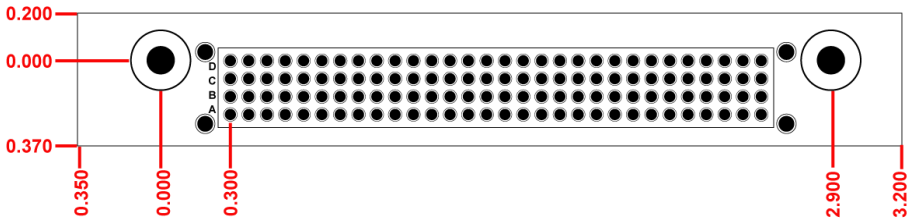


Figure 11.2-1: PC/104 Expansion Bus Connector Dimensions

PCI/104-Express Bus

The PCI/104-Express specification incorporates the PCI Express bus (PCIe) in addition to the previous-generation PCI bus. The specification defines a 156-pin surface mount connector for the PCI Express signals. The connector occupies the same location as the legacy PC/104 ISA connector on the board. In addition to PCI Express, the specifications also define pinouts on the connector that accommodate additional buses such as USB, SATA, and LPC.

The PCI/104-Express specifications define two pinouts for the PCIe connector: Type 1 and Type 2 described in Section: 11.3: PCIe/104 Type 1 and Type 2.

The PCIe bus connector is a surface-mount, not a through-hole connector. This makes it possible for a board to use different bus pinouts on the top side and the bottom side of the board. For example, a CPU board may have a Type 1 bottom PCIe connector and a Type 2 top PCIe connector. Such a CPU board would be compatible with Type 1 and/or Universal peripherals on the bottom, and compatible with Type 2 and/or Universal peripherals on the top.

PCI/104-Express incorporates Link Shifting functionality, which eliminates the need for the PCI slot selection switches/Jumpers found on PCI-104 and PC/104-Plus peripherals.

PCI/104-Express supports PCI Express and PCI.

PCIe/104 Bus

PCIe/104 is similar to the PCI/104-Express standard but without the legacy PCI bus. The PCI Express connector location and pinout options are identical to the PCI/104-Express Type 1 and Type 2 standards. A PCIe/104 board is incompatible with PC/104-Plus and PCI-104 systems –until a PCIe-to-PCI bridge device is used.

PCIe/104 supports PCI Express only.

11.3 PCIe/104 Type 1 and Type 2 Standards

There are two types of pinouts for the PCIe connector: **Type 1** and **Type 2**.

NOTE: The Elton baseboard supports Type 1 pinouts.

Type 1 offers four x1 PCI Express links, two USB 2.0 ports, and one x16 PCIe link. The pinouts follow the specifications specified for PCI/104-Express and PCIe/104.versions 1.0 and 1.1.

Type 2 offers four x1 PCI Express links, two USB 2.0 ports, two PCIe x4 links, two USB 3.0 ports, two SATA ports, and LPC. It replaces the PCI Express x16 link with two PCI Express x4 links, two USB 3.0, two SATA, LPC, and an RTC battery.

The OneBank implementation is compatible with Type 1 and Type 2 features.

CPU boards and peripherals may be designed as Type 1, Type 2, or Universal.

The Universal Type uses the common set of signals between the two types, PCIe x1 and/or USB 2.0.

Products introduced prior to 2011 will typically be either Type 1 or Universal.

The following table summarizes the comparison between Type 1 and Type 2 features of the module.

Feature	*Type 1*	*Type 2*	*OneBank*
USB 2.0	2		
SMB	1		
PCIe x 1	4		
Power	+3.3V, +5V, +12V	+3.3V, +5V, +12V	+3.3V, +5V
ATX Control	Yes	Yes	Yes
PCIe x 4		2	
PCIe x 16	1		
NOTE: x16 Link can be used as x8 or x4.			
USB 3.0		2	
SATA		2	
LPC		1	
RTC Battery		1	

11.4 PCI/104-Express Version 1.0 and 1.1 Host Board Compatibility

All host boards built on PCI/104-Express versions 1.0 and 1.1 are considered Type 1.

11.5 PCI/104-Express Version 1.0 and 1.1 Peripheral Board Compatibility

All PCI Express x1, USB 2.0, and SMBus boards build on versions 1.0 or 1.1 are considered Universal boards and are compatible with either, Type 1 or Type 2 hosts.

PCI Express x16 peripherals are compatible only with Type 1 hosts. USB 3.0, SATA, and LPC peripherals are compatible only with Type 2 hosts.

The pin assignments on Bank 1 of the connector are identical to Type 1 and Type 2 pin assignments, hence, all the PCI Express x1, USB 2.0, SMBus, and control signals are identical. The power and Ground signal functions operate the same way on the connector.

11.6 PCIe/104 Features

Connector A: PCI Express Bus

PCIe/104 Type 1, Type 2 and the OneBank implementation share the following features and pin assignments:

- Four x1 PCI Express Links
- Two USB 2.0
- ATX Power and Control Signals: +5V Standby, Power supply ON, Power OK, Power: +3.3V, +5V, +12V (A OneBank implementation does not include +12V)
- SMBus

Type 1 accommodates all the features listed under **Connector A: PCI Express Bus** and includes:

- One x16 PCI Express Link, or optionally two x8 Links, or two x4 PCI Express Links

Type 2 accommodates all the features listed under **Connector A: PCI Express Bus** and includes:

- Two x4 PCI Express Links Two USB 3.0
- Two SATA
- LPC Bus
- RTC Battery

11.7 PCI/104-Express Features

Connector A: Accommodates all the features listed under **Connector A: PCI Express Bus**

Connector B: High-Reliability Rugged Stacking Expansion Bus

PC/104 expansion modules can be mounted directly to the PC/104 bus connector.

Stacking connectors on the module, implement expansion buses for plugging boards vertically, empowering users to build modular embedded systems from board-level components.

An ISA compatible 32-bit PC/104 bus connector on the expansion module integrates 120 pins. It implements point-to-point general-purpose I/O interconnects, Switch-based technology, and Packet-protocol to deliver advanced features, such as Power Management, Quality of Service (QoS), Hot-Plug/Hot-Swap support, Data Integrity, and Error Handling.

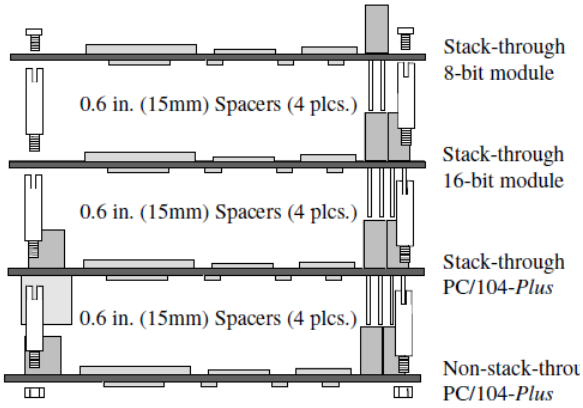
PCI/104-Express and PCIe/104 incorporate all required control and signal lines for ATX and power management functionalities. These signals include +3.3V, +5V, +12V, -12V and allow maximum power savings.

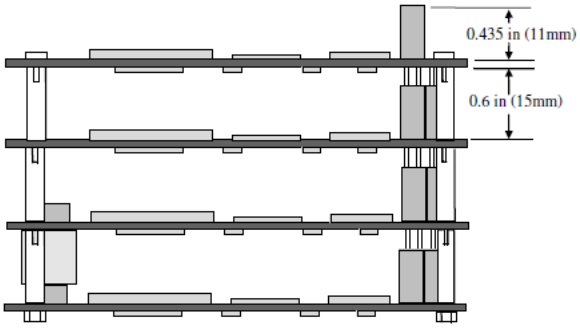
Stacking Third Party PC/104 Expansion Boards

As an open standard, PC/104 offers a robust platform on a global level that allows an extensive range of compatible boards, processors, expansion buses, CPUs, A/V controllers, I/Os, network interfaces, data acquisition boards, pin-and-socket connectors, operating systems, and software development tools to be integrated for high-end performance.

The maximum configuration for the PCI bus of PCI-104 modules is four boards plus the Host Board.

Typical side views of module stack configurations with dimensions are illustrated below.





High-Speed Data Transfer

The PC/104 architecture incorporates the PCI Express (PCIe/104 and PCI/104-Express, Generation 1 through Generation 4 versions) high-speed serial expansion bus that transfers data at rates shown in the table below.

The PC/104 interfaces the host computer using a 1-lane and an 8-lane PCI Express bus. Each lane operates at 8.0 Gbps (Gen 3). via the OneBank connector. The x8 lane PCIe port from The AGX Xavier Series Module is connected directly to the 2nd and 3rd Banks on the PCIe/104 connector.

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot.

The following table provides a summary of the PCI Express versions and their respective data transfer specifications.

PCI Express Version	*Transfer rate Gigatransfers Per Second*	*Bandwidth*	
		Per Lane	*X16 Lane Slot*
1.0	2.5 GT/s	4 Gbit/s (500 MB/s) 2 Gbit/s (250 MB/s)	32 Gbit/s (4 GB/s)
2.0	5 GT/s	4 Gbit/s (500 MB/s)	64 Gbit/s (8 GB/s)

11.8 PCIe/104 OneBank and PCI Express Connector

The PCI/104-Express OneBank is an extension of the existing PCI/104-Express/PCIe/104 standard developed by the PC/104 Consortium. that implements four x1 PCIe lanes along with other expansion bus functionalities in a high density, 52-pin connector for board-to-board stacking. It is a subset of the PCIe/104 3-bank bus, compatible with existing PCI/104-Express Type 1 and Type 2 modules.

The OneBank connector occupies the same slot as Bank 1 of the 3-Bank connector. Hence, OneBank signals include the same four x1 PCI Express Links, two USB 2.0, ATX power and control signals: +5V Standby, Power supply ON, Power Good, and Power: +3.3V, +5V (reduced current) as found on the first bank of the standard PCIe/104 bus making them plug-in compatible.

This preserves the stackability and compatibility of PCI/104-Express and PCIe/104 modules along with the new OneBank modules. By eliminating two of the banks, real estate on each side is extended. The speed levels up to PCIe Gen 3 on the PCIe/104 bus, generate higher bandwidth for future developments.

The following image represents the front top and bottom view of connector A OneBank and connector B PCI Bus.

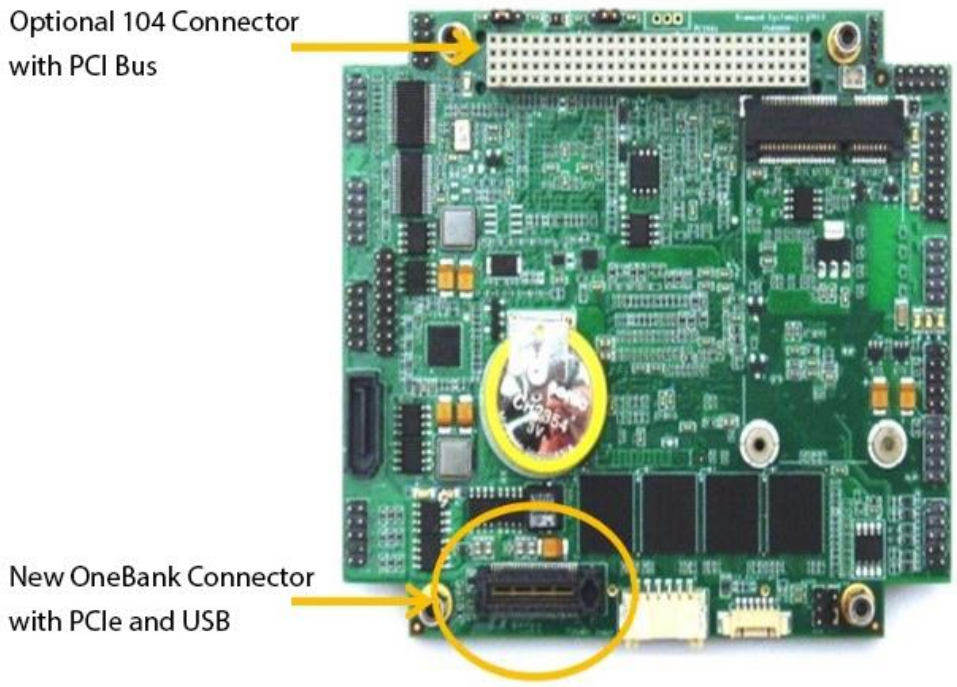


Figure 11.8-1: OneBank and PCI 104 Connectors

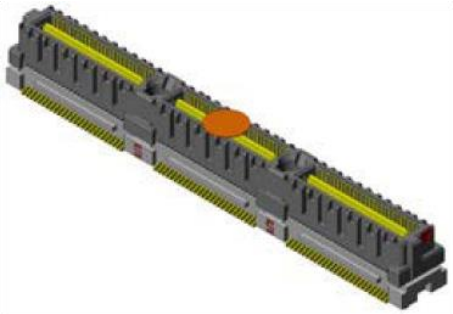
11.9 PCIe/104 3-Bank PCI Express Connector

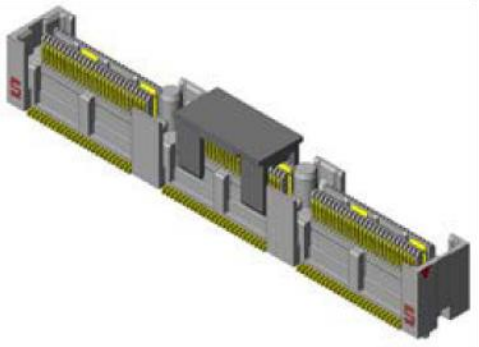
The standard PCIe/104 bus is designed for maximum bus feature functionality through a 152-pin 3-Bank connector which is classified as Type 1 or Type 2. Both Type 1 and Type 2 share a common feature set and pin assignments which include: Four x1 PCI Express Links, Two USB 2.0, ATX Power and Control signals: +5V Standby, Power supply on, Power Good, Power: +3.3V, +5V, +12V, and SMBus.

Type 1 implements an additional feature: one x16 PCI Express Link that can be configured as two x8 Links or two x4 PCI Express Links dependent on the host.

Type 2 implements the common feature set and two x4 PCI Express Links, two USB 3.0, two SATA, LPC Bus, and RTC Battery.

The following images represent the top and bottom views of Connector A with Pick and Place adapters.





11.10 Resources

Refer to the PC/104 Consortium site for the latest PC/104 specifications.

Refer to the PCI Special Interest Group: PCI-SIG site for the latest PCI and PCI Express specifications.

12. JUMPER DESCRIPTION

The Jumper blocks on the Elton baseboard can be configured to enable/disable or alter the default signal routing settings on the circuit, using Jumper shunts.

The following table describes the Jumper Blocks on the baseboard. Refer to Figure 6-1 for Jumper Locations.

Jumper	*Description*
JP1	LVDS BKLT, LVDS VDD, VIO PCI
JP2	Serial Termination, USB Host, LTE USB Selection
JP3	Serial Termination and PCI Power Disable

12.1 Input Voltage Selection: JP1

The baseboard accommodates an Input voltage selection Jumper, **JP1**, which enables input voltage signal sources to be selected and configured. Settings for Low-Voltage Differential Signaling Back Light (LVDS BKLT), Low-Voltage Differential Signaling Virtual Device Driver (LVDS VDD), can be configured. It can also be used to set the voltage supplied to VIO power pins for PC/104 cards.

NOTE: VIO voltage is used on most cards to supply the I/O Voltage for all PCI signals.

The following table describes Jumper Block **JP1** pinouts for LVDS BKLT, LVDS VDD, their designated functions and VIO PCI voltage settings. The text in bold and italics mark the default configuration on **JP1**.

Position	*Function*	*IN*	*OUT*
BKLT: 5V	LVDS Backlight	5V	-
BKLT: 12V	LVDS Backlight	***12V***	-
VDD: 5V	LVDS VDD	***5V***	-
VDD: 3V	LVDS VDD	3.3V	-
PCI: 3V	PCI IO Voltage	***3.3V***	-
PCI: 5V	PCI IO Voltage	5V	-

The following figure illustrates the default Jumper settings on the **JP1** block. The default Jumper positions are marked in red.

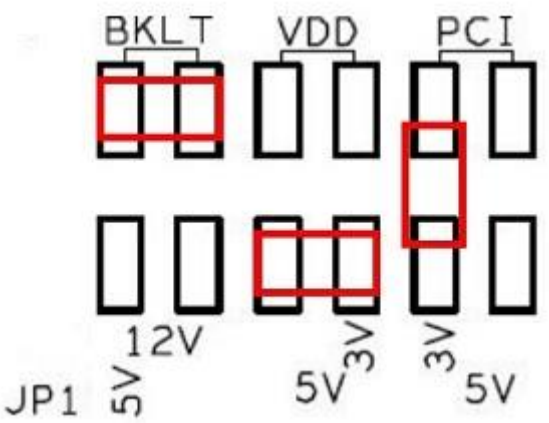


Figure 12.1-1: Jumper JP1 Default Location Settings

12.2 Serial Termination and USB Mode Selection: JP2

The **JP2** block settings can be switched/shorted to operate in different modes. The mode is selected using Jumper shunts. The options in **JP2** enable switching for the120ohm terminator resistor in the RS422/485 interface and the USB 2.0 ports.

The first four positions of the Jumper are used to select the termination points for serial ports 1 and 2 in the RS422/RS485 mode.

The fifth position of the Jumper will set the USB0 port to `HOST` mode or `Client` mode, which is the default setting.

The sixth position of the Jumper will set the USB routing to the LTE module, which is the default setting, or to the PCIe MiniCard.

The following table shows the pinouts, function and termination modes on the **JP2** block. The text in bold and italics mark the default configuration on **JP2**.

Position	***Function***	***IN***	***OUT***
1	Serial Port1 TX Termination	Enabled	Disabled
2	Serial Port2 TX Termination	Enabled	Disabled
3	Serial Port1 RX Termination	Enabled	Disabled
4	Serial Port2 RX Termination	Enabled	Disabled
5	USB 2.0 Port 0 on **J3**	***Host Mode***	Device Mode
6	USB 2.0 Port 3	***LTE Module***	PCIe MiniCard

The following figure illustrates the default Jumper settings on the **JP2** block.

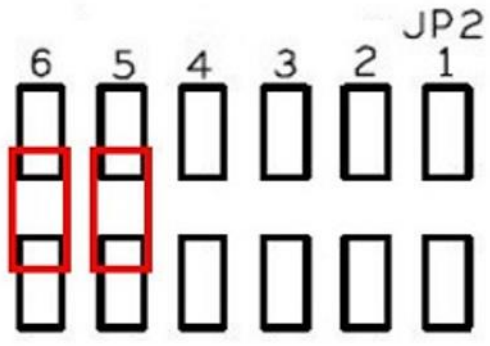


Figure 12.2-1: Jumper JP2 Default Location Settings

Note: On-board, numbers 1, 2, 3, 4, 5, and 6, indicate the location for a Jumper on pin numbers 1-2, 3-4, and 5-6, respectively.

12.3 Serial Termination Debug UART and PCIe/104 Power: JP3

The **JP3** block settings can be switched to operate in different modes.

- Serial Port 3 and Serial Port 4 TX Termination
- Serial Port 3 and Serial Port 4 RX Termination
- PCIe/104 Card Power Modes

The UART (Universal Asynchronous Receiver-Transmitter) interface on the microcontroller communicates with the serial ports to implement the debug console on the RS422/RS485 signaling standards.

The first four positions of the Jumper provide the termination points for serial ports 3 and 4 in the RS422/RS485 mode.

The fifth position of the Jumper will enable or disable the power supply to the PCIe/104 card.

The sixth position of the Jumper will select the debug UART or UART1 via serial port 1 on **J22**.

The following table specifies the pinouts, functions, and power modes for the **JP3** block. The text in bold and italics mark the default configuration on **JP3**.

Position	*Function*	*IN*	*OUT*
1	Serial Port3 TX Termination	Enabled	***Disabled***
2	Serial Port4 TX Termination	Enabled	***Disabled***
3	Serial Port3 RX Termination	Enabled	***Disabled***
4	Serial Port4 RX Termination	Enabled	***Disabled***
5	PCIe/104 Card Power	Disabled	***Enabled***
6	Debug Port via Serial Port1	Enabled	***Disabled***

The following figure illustrates the default Jumper settings on the **JP3** Block.

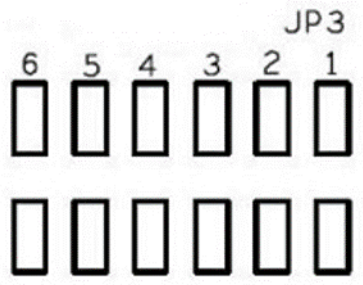


Figure 12.3-1: Jumper JP3 Default Location Settings

Note: On-board numbers 1, 2, 3, 4, 5, and 6, indicate the location for the Jumper on pin numbers 1-2, 3-4, and 5-6, respectively.

13. GETTING STARTED

This section covers the following topics:

- Information about the required components essential to install the hardware to flash the baseboard.
- Instructions to configure and setup the baseboard.
- Testing instructions to verify and confirm the installation process completed successfully.

13.1 Flashing Operating System to AGX Xavier Series Module

NOTE: The AGX Xavier Series Module must be programmed with the Diamond System Image file for the interfaces on the Elton baseboard to be operational.

Diamond Systems Image is released as a compressed ***tar.gz*** file, that can be unzipped on a Linux Host Machine and flashed on to the AGX Xavier Series Module.

To update the image on the AGX Xavier Series Module, Elton baseboard must be set to Recovery Mode. This is accomplished by pressing the **RCVRY** (**SW3**) button while powering up the baseboard.

Setting up the Hardware

1. Connect the cable number 6980603 to USB 2.0 port **J3**.
2. Connect the USB A2A cable to the 6980603 cable interface and the other end to the Host PC USB port.
3. Press the **RCVRY** (**SW2**) button while powering up the baseboard.

Refer to the following image for the display location of the **RCVRY** (**SW2**) button and the cable connections.

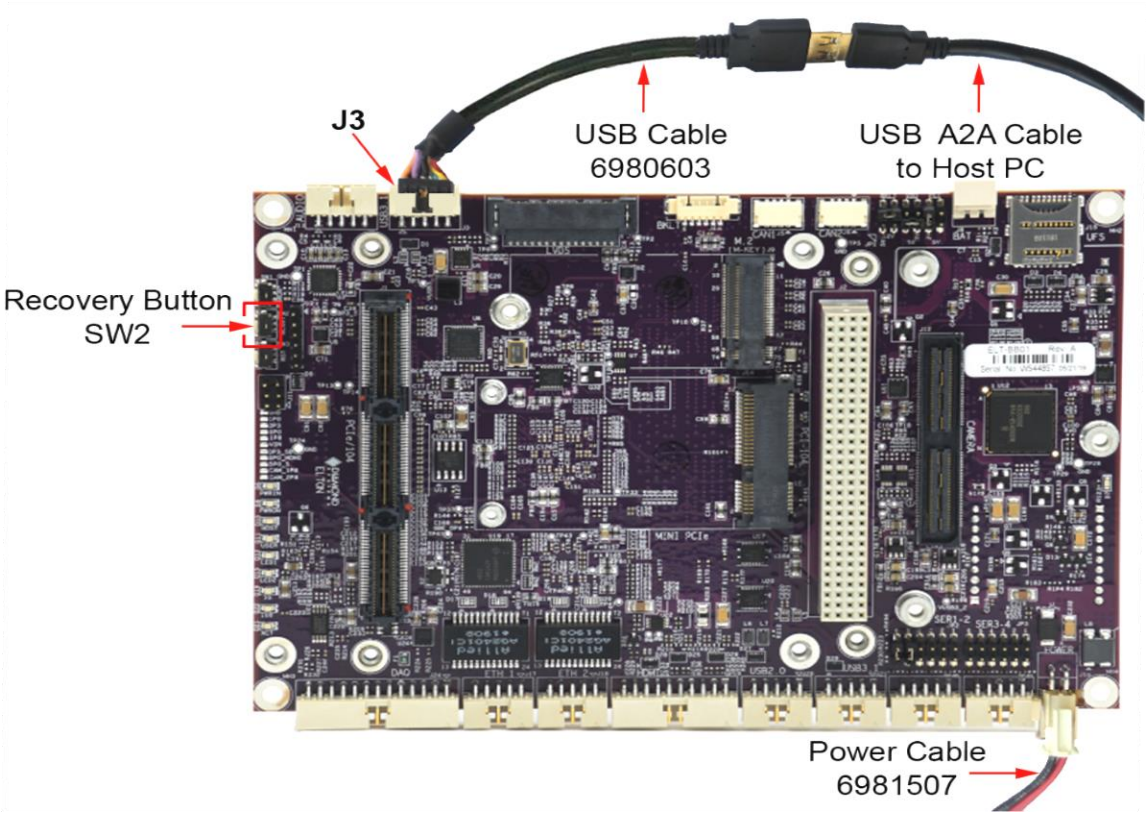


Figure 13.1-1: Setup to Initiate Recovery Mode on the Baseboard

NOTE: The sequence of images represented in this section have been captured from the Linux Host PC.

4. Download the Elton baseboard Image file `elton-release-0.1-20190627.tar.gz` file, from the FTP (File Transfer Protocol) site and copy it to the Linux Host Machine.

Figure 13.1-2: Elton Release Image File Displayed on Screen

To unzip the copied Image file:

5. Type and **Enter** the following command depicted in the Screen below. It may take a few minutes for the file to unzip.

```
sudo tar -pxvf elton-release-0.1-20190627.tar.gz
```

NOTE: The `tar.gz` file name is liable to change according to the version and release date.

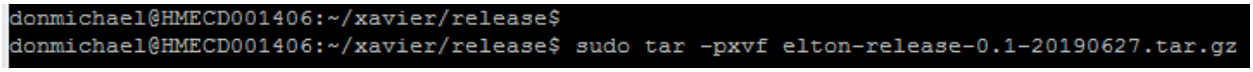


Figure 13.1-3: Image File to be Extracted Screen

To switch to the directory where the file has been extracted:

6. Type and **Enter** the following command as depicted in the Screen below.

```
cd Linux_for_Tegra
```

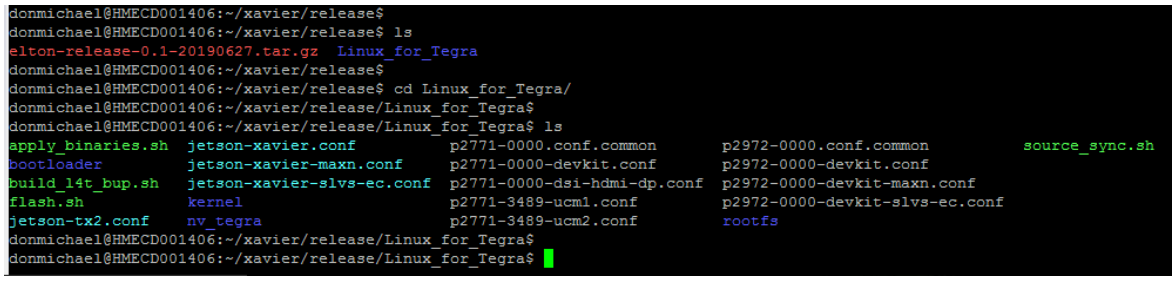


Figure 13.1-4: Image File Switch Directory Command Screen

To verify the baseboard is in Recovery Mode, in the Host PC running Ubuntu Operating System version 16.04 Terminal:

7. Type and **Enter**

```
lsusb.
```

The Terminal will display the NVIDIA device listed under USB devices as shown below.

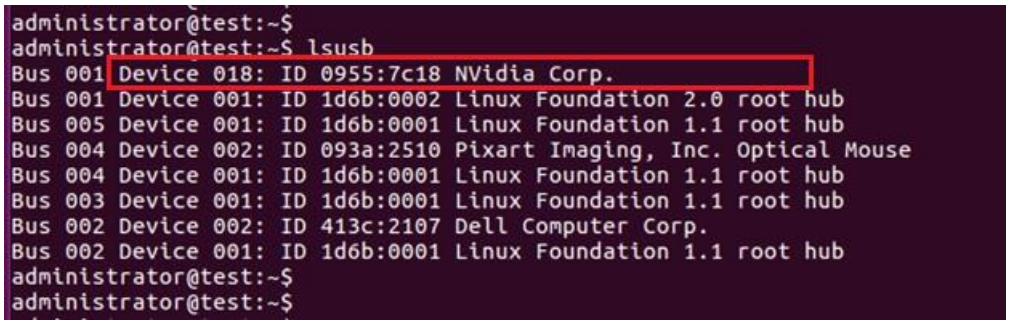


Figure 13.1-5: Device Detected on NVidia USB Bus Screen

To flash the AGX Xavier Series Module:

8. Type and **Enter** the following:

```
sudo ./flash.sh jetson-xavier-maxn mmcblk0p1
```

The flashing process will take 15-20 minutes to complete.

NOTE: Do not interrupt or interfere with the USB connectivity or the power supply to Elton until the flashing procedure is complete.

When the flashing is complete, the module will automatically Reboot.

On completion, a screen confirming a successful update to the module will be displayed as shown below.

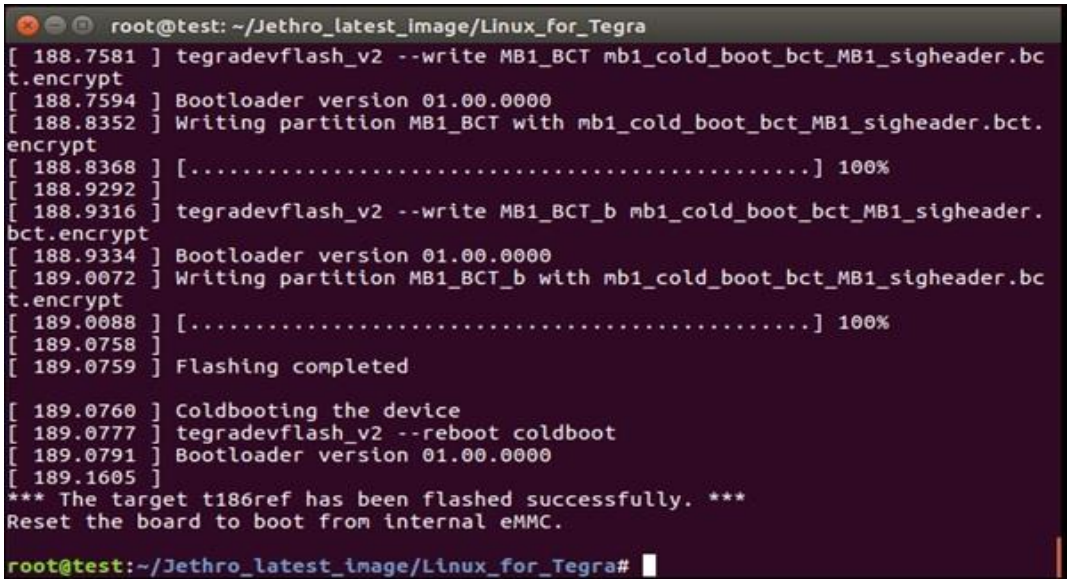


Figure 13.1-6: Notification on Task Completion Screen

9. Power cycle the baseboard.
10. Remove the FORCE RECOVERY mode connections when powered OFF during power cycle.
11. Continue testing after system Restart.

14. DATA ACQUISITION (DAQ) SUBSYSTEM

14.1 SAM Data Acquisition Circuit

Overview

Elton baseboard implements a data acquisition circuit with analog input, analog output, and digital I/O interfaces in conjunction with the NVidia Jetson AGX Xavier Series Module, which integrates a built-in DAQ subsystem supported by the Atmel SAM D51 Microcontroller Series Part No. ATSAMD51J18A from Microchip, to control and monitor “real world” devices.

A Programming Library provides resources for the development of custom applications along with a Graphical User Interface (GUI) that enables users to control the data acquisition I/O interface and data logging parameters.

Key features include:

- 6 Analog inputs, 0-3.3V input range, 12-bit resolution (1 part in 4096)
- 2 Analog outputs, 0-3.3V output range, 12-bit resolution (1 part in 4096)
- 13 Digital I/O (GPIO), 3.3V logic levels
- Miscellaneous board-specific controls

All DAQ I/Os are accessed on a 26-pin (2x13) 2mm pitch connector. Refer to Section: 8.16 Data Acquisition (DAQ) Connector: J24 for the pinout specifications.

The connector contains both analog and digital signals along with separate Grounds for each signal group. For noise cancellation procedures on the analog signals, all analog I/O connections must be referenced to the analog Ground pins 9 and 10, and all digital I/O signals must be referenced to the digital Ground pins 11 and 26.

A standard 2x13 2mm pitch ribbon cable connector or Diamond Systems non-latching cable No. 6980516 or latching cable No.6980606 can be plugged into the connector.

The Atmel SAM D51 microcontroller communicates with the AGX Xavier Series Module via a Serial Peripheral Interface (SPI) port. The SAM DAQ functions are controlled using the Programming Library included in the Elton baseboard’s operating system image files.

Refer to SAMD51 Software User Manual located at Diamond Systems Corporate GitBook site for detailed information.

14.2 Analog Inputs

Analog Input sensors convert a voltage level signal into a digital value that can be analyzed, stored, and controlled.

The six analog inputs feature a 12-bit native resolution and single-ended 0-3.3V input range. The microcontroller is configured to use an external 3.3V reference voltage provided by a reference voltage IC on the board for improved accuracy.

Analog Input	
No. of Channels	6 Single-Ended or 3 Differential Inputs
Resolution	0x00112-bits (1 part in 4096) Native Up to 16-bits with Software Averaging
Input Voltage Range	0-3.3V
Sample rate	Maximum 1 KHz Using Diamond System Programming Library

Warning! There is no built-in protection circuitry on the analog inputs. Input voltages above the 3.3V maximum range may cause damage to the SAM microcontroller.

Although the native A/D resolution is 12-bits, the SAM microcontroller contains an innovative feature that enables higher resolution by averaging several samples. This technique enables the resolution to be configured to 16-bits.

Oversampling and averaging can be used to:

- Increase measurement resolution.
- Improve the Signal-to-Noise Ratio (SNR) and measurement resolution reduced throughput.
- Improve SNR for “white” noise.
- Reduce noise while maintaining a 12-bit resolution.

The disadvantages of averaging samples are an increased CPU utilization that results in each individual A/D measurement taking longer to compute and a reduced maximum sampling rate.

NOTE: Averaging is supported by the Programming Library.

The analog inputs can be configured in either single-ended or differential mode.

The pinouts for the mapping for input channels in differential mode are specified in Table 14-1: I/O Signal Mapping.

For a single-ended input, the input voltage on the input pin is measured in comparison to the analog Ground pin on the I/O connector.

NOTE: It is recommended to avoid using digital Ground pins for analog input measurements since it will display a higher noise-level and result in less accurate readings.

In a differential input, the voltage measurement is the value between the high and low input channels.

NOTE: In differential mode, the A/D value will not yield a measurement lower than 0V, corresponding to an A/D code of 0. In this scenario, the inputs may be considered to be “pseudo-differential”. A differential input is useful if the sensor or device being measured is far from the board or is powered by a different power supply wherein the Grounds of the two systems may differ.

A more accurate measurement can be obtained by connecting the Ground of the device being measured to the low channel on the SAM circuit, and the input signal to the high side.

The 12-bit resolution refers to the conversion of an analog voltage to a digital value in 12-bit integers.

The circuit can measure the input voltage with an accuracy of 3.3V / 4096 or approximately 0.81mV. The conversion formulas between the input voltage and A/D code shown below, are based on the ideal case scenario.

A/D Conversion Formulas:

A/D code = input voltage / 3.3V x 4096 (min value 0, max value 4095)

Input voltage = A/D code / 4096 x 3.3V

The following table uses specific data for input voltage and A/D values based on the ideal case scenario.

NOTE: Based on convention, the top end of the 3.3V range should correspond to a code of 4096, which requires 13-bits. Therefore, the maximum A/D code of 4095 corresponds to 1 LSB less than 3.3V as shown in the following table.

Vin	*A/D Code Hex*	*A/D Code Dec*
0.0000V	0x000	0
0.0008V	0x001	1
0.0016V	0x002	2
0.0016V	0x002	
1.6592	0x7FF	2047
1.6500V	0x800	2048
1.6508V	0x801	2049
1.6508V	0x801	2049
3.2992V	0xFFF	4095

All A/D circuits are susceptible to inherent gain and offset errors depending upon factors such as temperature. The SAM circuit calibrates some of these errors to provide better accuracy.

The Diamond Systems driver and Programming Library calibrate raw uncorrected data or corrected data with greater accuracy between the A/D input range of 0V and/or 3.3V.

NOTE: Due to the inherent characteristics of the microcontroller regarding accuracy readings, the full input range of 0-3.3V may not be attainable.

In some scenarios, the minimum measurable voltage maybe a few millivolts above 0V, and the maximum measurable voltage maybe a few millivolts below 3.3V. In other scenarios, the corrected A/D measurement may exceed 0V or 3.3V.

This is due to software calculations which computes a straight line based on offset and gain calibration measurements. These extended voltage readings are correct.

A/D sampling can be performed one channel at a time or in a “scan” of multiple consecutive channels.

In a scan, a small-time delay exists between each sample, because the microcontroller converts the input voltages individually. The interval between the samples is approximately 1us. Additionally, interrupt processing can be used to manage a steady stream of A/D samples without the software monitoring each sample continuously.

A FIFO (First-in, First-out) in the SAM microcontroller stores A/D samples and forwards them to the main processor in chunks at regular intervals.

Refer to the Programming Reference Manual for more details on A/D sampling methods.

14.3 Analog Outputs

Analog Output sensors convert digital values into analog voltages or current signals that can be analyzed and controlled.

A single-ended output is a signal that is always referenced to the shield -which is typically earth Ground, on the output connector. The voltage should be measured in proportion to the analog Ground pins.

The two analog outputs feature a 12-bit resolution and single-ended 0-3.3V output range.

Analog Output	
No. of Channels	3 Single-Ended
Resolution	0x00112-bits (1 part in 4096) Native
Output Voltage Range	0-3.3V
Maximum Current	Refer to the SAM D5x/E5x Family Data Sheet for details.

NOTE: Do not use the digital Ground pins for analog output measurements since it has a higher noise-level and will result in poor quality output voltage signals.

The 12-bit resolution refers to the output of the requested voltage in 12-bit integers with an accuracy of 3.3V / 4096 or approximately 0.81mV. The conversion formulas between D/A code and output voltage shown below are based on the ideal case scenario.

D/A Conversion Formulas

D/A code = desired output voltage / 3.3V x 4096 (min value 0, max value 4095)

Output voltage = D/A code / 4096 x 3.3V

The following table uses specific data for input voltage and A/D values based on the ideal case scenario.

NOTE: Based on convention, the top end of the range (3.3V) must correspond to a code of 4096, which requires 13-bits. Therefore, the maximum D/A code of 4095 corresponds to 1 LSB less than 3.3V as shown in the table below.

D/A code Hex	***D/A code Dec***	***Output voltage***
0x000	0	0.0000V
0x001	1	0.0008V
0x002	2	0.0016V
0x7FF	2047	1.6592
0x800	2048	1.6500V
0x801	2049	1.6508V
0xFFE	4094	3.2984
0xFFF	4095	3.2992V

14.4 Digital I/O Operations

The DAQ circuit contains 13 digital I/O (GPIO) lines with 3.3V logic levels. During power-up or reset, all I/O lines are programmed to input direction to avoid any conflicts with external circuitry.

Each digital I/O line can be individually configured to set the input or output direction. This enables the lines to split between input and output. All lines can also be individually read or written or read in groups by port. Port A consists of 8 lines A0-A7, and Port B consists of 5 lines B0-B4.

14.5 Miscellaneous Functions

The SAM circuit administers several other circuits and features on the board. These features are controlled using the Programming Library that contains specifics on using the special-purpose I/O pins.

Power Supply Monitor

The SAM circuit uses four additional analog inputs to measure the on-board power supply voltages. In certain scenarios, the A/D reading needs to be multiplied by a scale factor to derive the actual voltage.

User LED Function

The circuit provides a LED connection tied to a GPIO line that is fully-functional and can be controlled by the software to monitor the circuit.

Peripheral Control

The peripherals listed below are administered by the Atmel SAM D51 microcontroller. The available features vary from carrier board to board.

Refer to the Programming Reference Manual for details on each peripheral.

- Fan Enable/Disable (connected to the fan connector)
- LTE Module Enable
- HDMI 5V Power Enable
- Camera Power Control
- Serial Port Protocol Configuration

Temperature Monitor

The Atmel SAM D51 microcontroller contains a temperature monitor that reports the temperature of the chip in degrees Celsius. This is useful in obtaining information on the overall ambient temperature of the carrier board environment.

I/O Signal Mapping

NOTE: The specifications provided in the following table are for reference purposes only.

The pinout descriptions and their functions specified in the following table are derived from the Atmel SAM D51 Microcontroller Package No. TQFP-64 and are applicable when using the microcontroller.

The pinout specifications in the table do not apply to the Diamond Programming Library functions since the mapping functions are managed by the software.

Table 14-1: I/O Signal Mapping

SAM Pin No.	SAM Pin Name	DAQ Function
13	PA04 / ADC0_AIN4	ADC0 / ADC0-
12	PB09 / ADC0_AIN3	ADC1 / ADC0+
11	PB08 / ADC0_AIN2	ADC2 / ADC1-
16	PA07 / ADC0_AIN7	ADC3 / ADC1+
15	PA06 / ADC0_AIN6	ADC4 / ADC2-
64	PB03 / ADC0_AIN15	ADC5 / ADC2+
3	PA02 / DAC_VOUT0	DAC0
14	PA05 / DAC_VOUT1	DAC1
1	PA00	GPIO A0
63	PB02	GPIO A1
62	PB01	GPIO A2
61	PB00	GPIO A3
60	PB31	GPIO A4
59	PB30	GPIO A5
51	PA27	GPIO A6
50	PB23	GPIO A7
49	PB22	GPIO B0
46	PA25	GPIO B1
45	PA24	GPIO B2
44	PA23	GPIO B3
43	PA22	GPIO B4
17	PA08	5.0V Rail; Scale Factor 2.0
18	PA09	Main Input Voltage; Scale Factor 5.525
19	PA10	1.8V Rail; Scale Factor 1.0
20	PA11	3.3V Rail; Scale Factor 2.0
35	PA16	User LED
23	PB10	Fan enable
24	PB11	LTE module enable
39	PB16	HDMI 5.0V enable
40	PB17	WLAN disable#
36	PA17	Camera 1.2V enable (Active Low)
37	PA18	Camera 1.8V enable (Active High)
38	PA19	Camera 2.8V enable (Active High)
41	PA20	Serial Ports 1-2 Config bit 0
42	PA21	Serial Ports 1-2 Config bit 1
32	PA15	Serial Ports 1 & 2 Slew Rate

15. THERMAL SOLUTIONS

The Elton baseboard implements an optimized Thermal Management System to ensure that the baseboard and components are maintained at their maximum specified temperatures. Applying a thermal management component below recommended standards will produce undesirable consequences.

The baseboard is designed to operate at a temperature range of-40°C to +85°C, while the AGX Xavier Series Module operates at a temperature range of -25°C to +80°C. To ensure compatibility and circumvent the difference in operating temperatures, the AGX Xavier Series Module integrates a Product-Level Thermal Transfer Plate (TTP) as a Thermal Solution which can accommodate the following solutions:

- Passive Heat Sink
- Active Heat Sink
- Cold Plate
- Chassis Mount or similar component

The Thermal Solution to be implemented interfaces the NVIDIA TTP. To ensure proper implementation, Customers are required to follow the specified standards stated in NVIDIA's JETSON AGX XAVIER Thermal Design Guide before implementing thermal solutions for the AGX Xavier Series Module and module-specific Thermal Transfer Plate (TTP).

NOTE: The user must be logged in to the developer.nvidia.com site to access the ***JETSON AGX XAVIER Thermal Design Guide***.

The Thermal Solution must be attached to the top surface of the TTP. However, based on the chassis design, many configurations are possible. For typical scenarios the following recommendations are applicable:

- The contact of the thermal solution must be well administered on the TTP.
- NVIDIA thermal testing has demonstrated that the maximum specified TTP temperature controls the temperature range of all components on the baseboard.

To determine the best method to interface the TTP with the respective Thermal Solution and ensure thermal, mechanical and qualification compatibility at the system-level, refer to NVIDIA's ***JETSON AGX XAVIER Thermal Design Guide*** mentioned above for details on specifications.

The following table provides the specifications for the AGX Xavier Series Module.

Parameter	***30 W Mode[1]***	***MaxN Mode[2]***	***Unit***
Maximum TTP Operating Temperature[3]	80	80	°C
Recommended Xavier Module Operating Temperature Limit[4]	T.cpu = 90.0	T.cpu = 86.0	°C
	T.gpu = 92.5	T.gpu = 88.0	°C
	T.aux = 89.0	T.aux = 82.0	°C
Xavier Module Maximum Operating Temperature Limit[5]	T.cpu = 95.5	T.cpu = 91.5	°C
	T.gpu = 98.0	T.gpu = 93.0	°C
	T.aux = 94.5	T.aux = 87.5	°C

[1] The Power Management for Jetson AGX Xavier document describes multiple power modes: a 10 W, a 15 W, and several 30 W modes. The same temperature settings apply to all of these power modes that are within the 30 W module power budget.
[2] The MaxN power mode allows for higher operating power levels. These higher power modes require lower temperature limits to maintain the reliability of Jetson AGX Xavier.
[3] The temperature of the TTP must always be kept within this 80 °C limit to maintain the specified performance and reliability. The measurement locations are provided in Figure 3-2 of the JETSON AGX XAVIER Thermal Design Guide.
[4] These are the temperature thresholds below which the product will operate at the specified clock speeds. See Section 4.3 of the JETSON AGX XAVIER Thermal Design Guide.
[5] The Xavier SoC will reset the Jetson AGX Xavier Module once any of these software-imposed temperature limits are reached to maintain the reliability of the Xavier SoC. See Section 4.5 of the JETSON AGX XAVIER Thermal Design Guide.

15.1 Baseboard Heat Spreader Specifications

Elton baseboard accommodates a Heat Spreader that transfers energy from the hotter source to a heat sink or heat exchanger and contains high thermal conductivity. It is designed to dissipate heat effectively for optimal thermal performance and optimize performance while maintaining the baseboard rated temperature.

The Heat Spreader material is manufactured under high temperature and high-pressure sintering of particles to form a lattice structure that is placed intermediate between heat spreading materials. The fine grain crystal structure is uniformly distributed to enable heat dissipation.

The following Schematic represents the bottom view of the Heat Spreader installed on the baseboard.

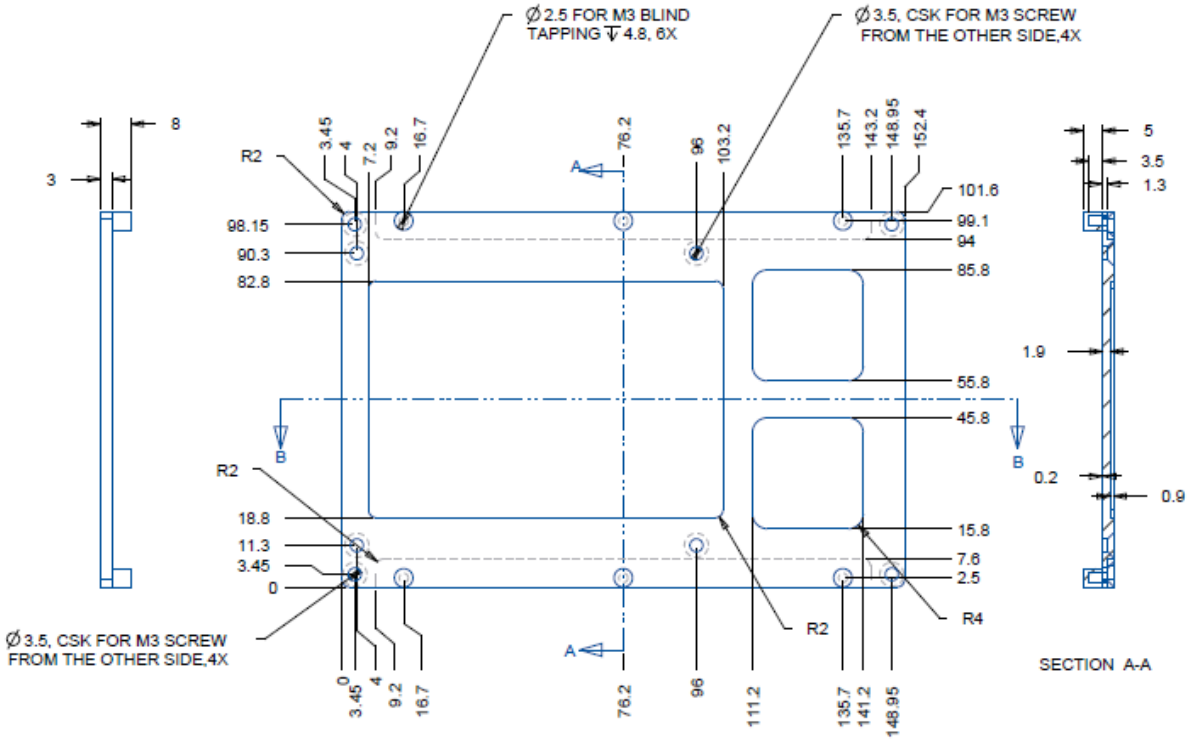


Figure 15.1-1: Schematic Bottom View of the Heat Spreader

The following image illustrates the Outer and Inner Mounting Holes on the baseboard and for the AGX Xavier Series Module Thermal Accessory.

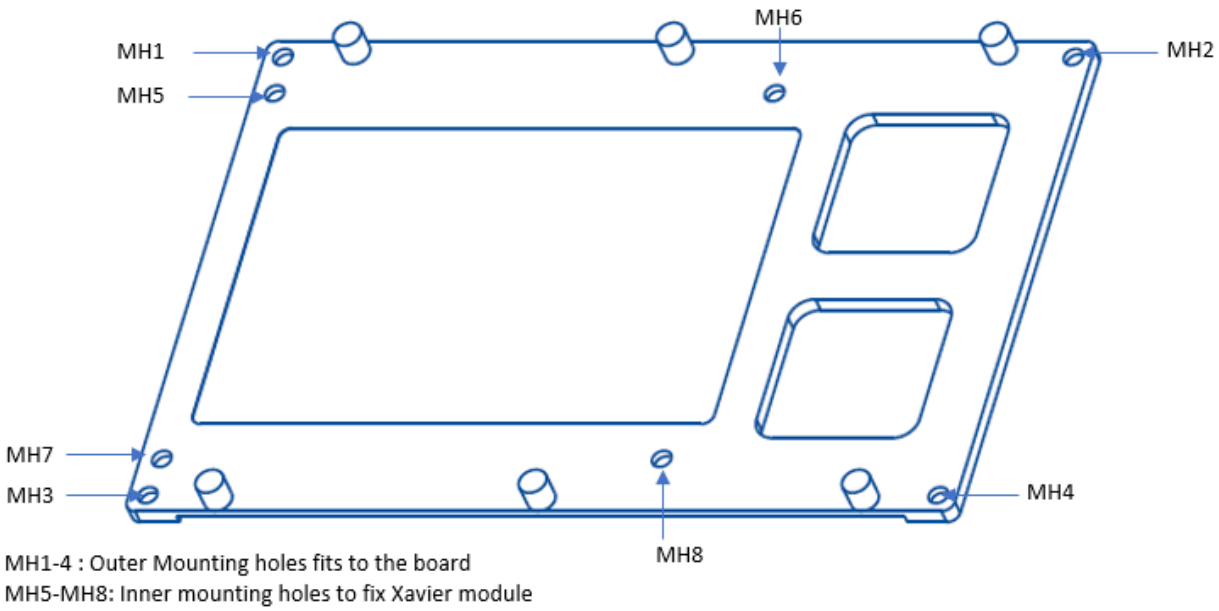


Figure 15.1-2: Schematic Top View Section with Mounting Hole Specifications

The following image depicts the baseboard with the Heat Spreader installed.

Figure 15.1-3: Baseboard with Heat Spreader Plate Installed

16. SPECIFICATIONS

The Elton baseboard Specifications are summarized in the following table.

Feature	
Module	AGX Xavier Series
CPU	8-Core ARM v8.2 64-Bit CPU, 8 MB L2 + 4 MB L3
Cooling Accessory	Heat Spreader
SDRAM Memory	1 6GB 256-bit LPDDR4x; 2133MHz – 137 MBGB/s
Display	Three Multi-Mode DP 1.2/eDP 1.4/HDMI 2.0
USB Ports	2x USB 2.0, 2x USB 3.1
Serial Ports	4 RS-232/422/485 Ports
DAQ	13 Digital I/Os; 6x SE ADC Input or 3x DE ADC Input; 2x DAC Output
Camera	4x MIPI CSI-2 x4 Lane Each
Connectivity	2 x 10/100/100 Mbps Ethernet, 1x NimbeLink Skywire® 4G LTE
Mass Storage	1 M.2 PCIe SSD, 1 Micro SD and UFS Card
Expansion Bus	PCIe/104 3 Bank (4Nos x1 PCIe, 2x USB 2.0, 1No x8 PCIe), PCI-104 via PCIe to PCI Bridge, 1 Mini PCIe Full Size Card
Utility	PWR_BTN, RESET, FORCE RECOVERY
Digital/Analog Specifications	
Number of Lines	13
Direction	Programmable Bit by Bit
Input voltage	
Logic 0:	0.0V Min, 0.99V Max, ±1uA
Logic 1	2.31V Min, 3.3V Max, ±1uA
Output Voltage	
Logic 0:	0.0V Min, 0.66V Max, +8mA (Typical)
Logic 1	2.64V Min, 3.3V Max, -8mA (Typical)
Analog Inputs	
Number of Inputs	6; Single-Ended or Differential
A/D Resolution	12-bit Resolution (1 Part in 4096);
Input Voltage Range	Single-Ended 0-3.3V
A/D sampling	One or Consecutive Channels
Analog Outputs	
Number of Outputs	2; Single-Ended
D/A Resolution	12-bit Resolution
Output Voltage Range	3.3V x 4096 (Min Value 0, Max Value 4095)
Mechanical and Environmental Properties	
System Input Voltage	+9VDC +/-5% to +20VDC +/-5%
Power Consumption	~30W
Dimensions	4”x6” (101.6mm x 152.4mm)
Weight	183.6 Grams (6.47 Ounces) Without Heat Spreader
Operating Temperature	-25°C To +80°C (-18°F To +176°F)
Shock	MIL-STD-202G Compatible
Vibration	MIL-STD-202G Compatible
RoHS	Compliant

17. ADDENDUM

The following section provides additional information and instructions relevant to the components specified in the Main Sections of this document.

17.1 Programming NXP PTN3460 Chip

NOTE: Conventionally, the PTN3460 chip is packaged pre-programmed by the integrated circuit manufacturer. The following instructions have been provided as an additional resource.

The LVDS interface can be configured using multi-level configuration pins (CFG1, CFG2, CFG3, and CFG4) or through the Register interface.

The register interface provides a greater level of flexibility in configuring parameters relevant to LVDS output swing, spreading depth and more, than the multi-level configuration parameters available on pins.

The PTN3460 integrates a register interface that can be accessed by CPU/GPU or System Controller to configure and customize settings. The registers can be read/written to, either via DP AUX or I2C-bus interface. The register settings override the pin values.

All registers must be configured during power-on initialization after the HPDRX pin pulse is HIGH.

By default, the GPIOs for PTN3460 are in Power-Down mode and must be programmed to Power-Up by invoking a script session using the following script.

```
home/nvidia/lvds-en.sh
```

Enter the following command lines in the terminal to run the script.

```
cd /home/nvidia
sudo ./lvds-en.sh
```

Using the **sysfs** interface, enter the following command lines:

```
#sudo su
#echo 490 > /sys/class/gpio/export
#echo out > /sys/class/gpio/gpio490/direction
#echo 1 > /sys/class/gpio/gpio490/value
```

The `/sys/class/gpio/export` string exports a GPIO pin based on the pin name/number entered in the string and makes it visible in the sysfs file system.

The `/sys/class/gpio/gpio490/direction` string sets the GPIO direction to in/out. If it is an output pin, the command sets the level to low or high.

The `/sys/class/gpio/gpio490/value` string sets the GPIO output value to 0/1 (low or high).

Using I2Ctools

The LVDS functionality is implemented through the eDP to PTN3460 LVDS bridge interconnectivity.

For the display screen to transmit LVDS signals, it must be capable of communicating with the video source. EDID (Extended Display Identification Data) structures the data for the display using EDID communication protocols.

The DP AUX interface on the PTN3460 transports i2c (Inter-Integrated Circuit}-over-AUX commands and supports EDID-DDC communication with the LVDS panel. To support panels without EDID ROM, the PTN3460 can emulate EDID ROM behavior.

The i2c address on the PTN3460 chip is 0x20 and resides on Bus 2.

The following Read and Write commands enable the user to access and control data that is stored in registers. In order to transact write byte/read byte, the register must be specified.

The GPIOs for PTN3460 can be programmed through i2c communication bus connected to the Xavier Series Module as described in the parameters below. The I2Ctools to program PTN3460 chip are included in the BSP (Board Support Package).

Write Command Parameters

The `i2cse command` is a method to set register visibility through the i2c bus.

To write to a register, enter the `i2cset` command line as follows:

```
#sudo i2cset -y -f <bus no> <device address> <register address> <data>
```

For example, to write `0x01` to `0x80`, the syntax would be as follows:

```
#sudo i2cset -y -f 2 0x20 0x80 0x01
```

The following table describes the command parameters.

Command	***Description***
`i2cset`	Write data to an i2c device.
`[-f] [-y]` Options	`-f` forces access to the device if the device is in a busy mode. May return an invalid value.
	`-y` disables interactive mode and bypasses prompts for confirmation from the i2cget command. By default, it will wait for user input before interacting with the i2c device.
`<bus no>`	Value of the i2c bus. Indicates the number of the i2c bus to be scanned.
`<device address>`	Specifies the address of the chip on the specific bus.
`<register address>`	Specifies the address on the chip to write to.
`<data>`	Parameters to be written for the device.

Read Command Parameters

The `i2cget` command is a method to read a byte from a specified register on the i2c device. To read from a register, enter the i2cset command line as follows:

```
#sudo i2cget -y -f <bus no> <device address> <register address>
```

For example, to retrieve and read `0x01 to 0x80`, the syntax will be as follows:

```
#sudo i2cget -y -f 2 0x20 0x80
```

To retrieve and read complete data from the register, the syntax will be as follows:

```
#sudo i2cdump -y -f 2 0x20
```

The image below depicts the screen dump of a programmed PTN for M215HTN01.1 LCD with dual-channel at 1920x1080 resolution.

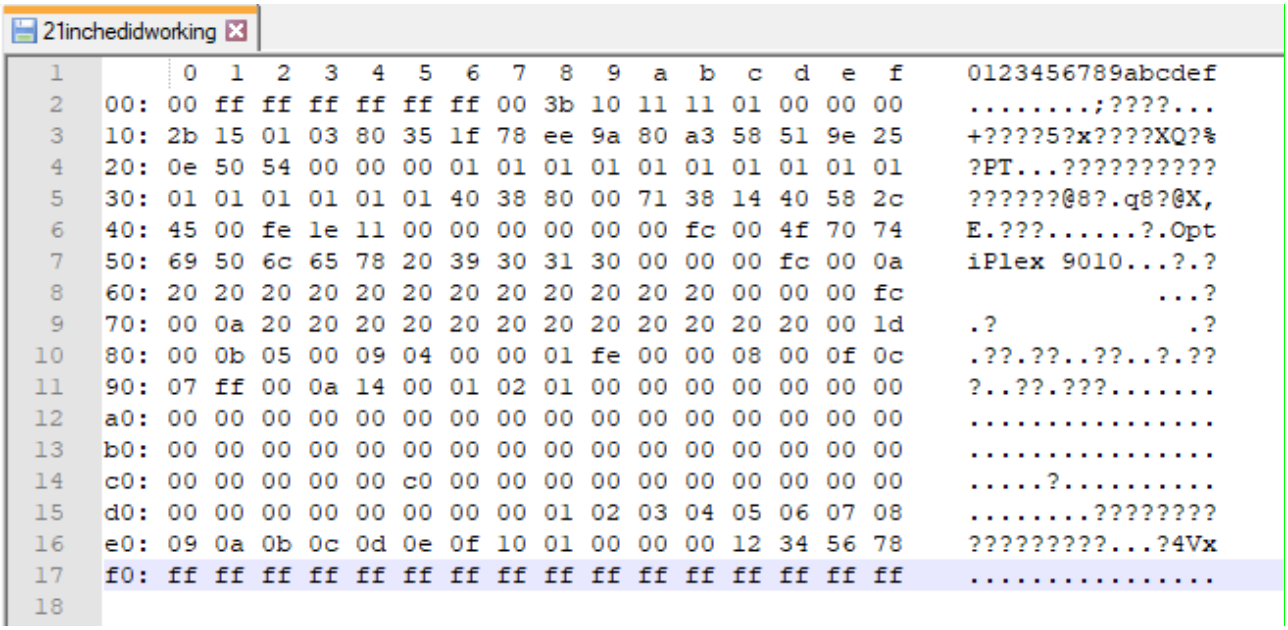


Figure 17.1-1: Screen Dump PTN for M215HTN01.1 LCD Display with Dual Channel

The registers for Read and Write operations for the LVDS bridge IC PTN3460 device and the baseboard are addressable at a range of Type Values 0x80-0x8F.

NOTE: It is recommended to compare all registers ranging from 0x80 to 0x8F and program the PTN3460 chip accordingly.

Once the programming is complete, the PTN3460 chip must be flashed. To execute flashing the following sequence must be used, where the Default Values must be replaced with the Offset (Hex) Values as specified in the table below.

Default Value	*Offset (HEX)*	*Size (bytes)*	*Name*	*Bit Field*	*Note*
0xE8	0x01	1	Flash Command	7:0	Flash Operation to be Executed (Default 0) 0 - Erase Only 1 - Erase and Flash
0xE9	0x78	2	Flash Magic Number	7:0	Must be Equal to 0x7845 for Flash Command to be Processed (Big Endian) (Default 0)
0xEA	0x45				The 0xEA is a Hexadecimal format error code used to identify the error caused. The 0x45 is an error-diagnostic scan code.
0xEB	0x56	1	Flash Trigger	7:0	Must be Equal to 0x12345678 for PTN3460 to Consider Flashed Configuration Table (Big Endian) (Default 0)

When the Flashing process is complete:

- Power cycle the system and verify that the PTN3460 chip has retained the written values.
- Set the GPIO to high-level mode.

Refer to Section 17.1 Programming NXP PTN3460 Chip for scripting instructions on setting the GPIO to high-level mode.

For other LVDS resolutions, refer to the respective display datasheets and set the registers accordingly.

17.2 Camera Installation Procedures

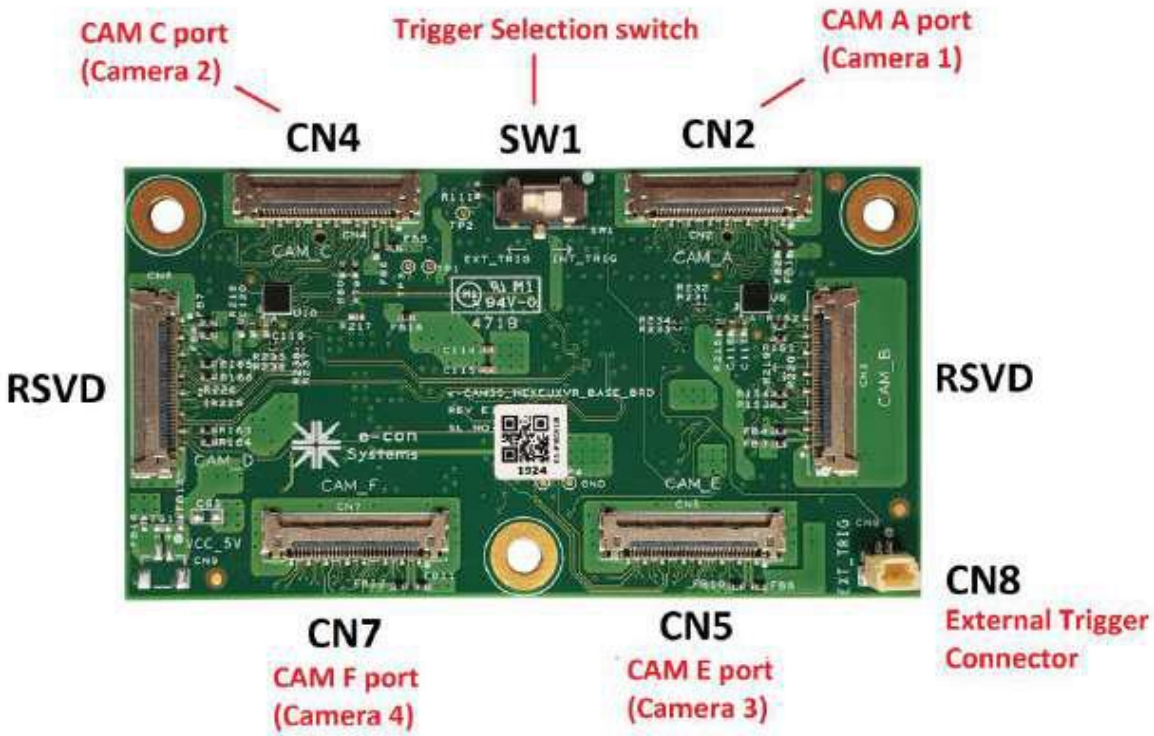
Similar to the Xavier Developer Kit Carrier Board, the Elton baseboard supports four MIPI CSI x4 camera interfaces through a 120-pin daughterboard connector.

Synchronized-4k-cameras from e-con Systems™ can be plugged into the daughterboard connector to support the four 4-lane or six 2-lane cameras. The daughterboard connector also supports i2c and control signals which enable users to directly interface the camera to the baseboard.

The following procedures use the e-CAM130_CUXVR MIPI-four-AR1335-module camera board to demonstrate the installation and implementation of the cameras. The prebuild module drivers provided in the e-CAM130_CUXVR package are loaded automatically during the boot.

The e-CAM130_CUXVR is a multi-board set comprising of three board components as follows:

1. **The Camera Baseboard** (e-CAM30_HEXCUXVR_BASE_BRD)



Refer to the ***e-CAM130_CUXVR_Getting_Started_Manual.pdf*** on the Documents page located at the e-con Systems site for detailed interfacing information.

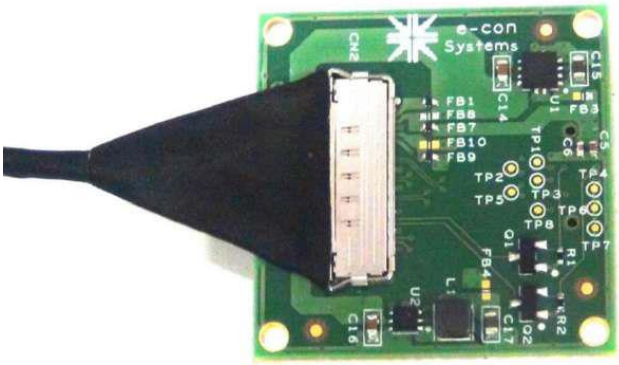
2. **The Adaptor Board** :
   e-CAM130_TRICUTX2_ADAPTOR

3. **The Dual Board**
   e-CAM137_CUMI1335_MOD

1. Insert the e-CAM130_CUXVR board CN1 connector to the camera connector on the Elton baseboard. Refer to Section 6: Connector And Jumper Location. for the location of the camera connector.
2. Interface the four adaptor boards to the baseboard using the supplied four micro-coaxial cables.
3. Connect the micro-coaxial cable to the adaptor board connector and baseboard connector as depicted below.

The images of the micro-coaxial cable and the cable connected to the Adapter Board are shown below.

Micro-Coaxial Cable



Micro-Coaxial Cable Connected to The Adaptor Board Connector

4. Lock the position of the cable on the baseboard.
5. Connect and lock the remaining three cameras as specified in Steps 1 through 4 above.

An image of the 4-camera installation is depicted below.

6. Power-on the system.

NOTE: For a successful implementation ensure that the trigger signal range conforms to 3.3V or 5V. A voltage signal greater than 5V will cause permanent damage to the chip.

The synchronous mode is a special feature of the e-CAM130_CUXVR board that synchronizes all the captured camera frames according to the integrated PWM pulse within the trigger functionality. This PWM trigger pulses can be implemented internally using the Internal Trigger Mode, or externally using the External Trigger Mode.

7. Switch **SW1** to **EXT_TRIG** position when providing **PWM** trigger signal from an external source. When using an internal **PWM** trigger signal, the **SW1** switch must remain in the **INT_TRIG** position This calibrates frames in a synchronous mode.

8. Enter the following command line to access the cameras and begin the streaming process:

```
gst-launch-1.0 v4l2src device=/dev/video0 ! "video/x-
raw,format=(string)UYVY, width=(int)3840, height=(int)2160" !
nvvidconv ! "video/x-
raw(memory:NVMM),format=(string)I420,width=(int)1920,
height=(int)1080" ! nvoverlaysink overlay-w=1920 overlay-h=1080
sync=false
```

When the command is executed the following screen will be displayed.

```
nvidia@jetson-0420119049088:~$ gst-launch-1.0 v4l2src device=/dev/video1 ! "video/x-raw,format=(string)UYVY, width=(int)3840, height=(int)2
160" ! nvvidconv ! "video/x-raw(memory:NVMM),format=(string)I420,width=(int)1920, height=(int)1080" ! nvoverlaysink overlay-w=1920 overlay-
h=1080 sync=false
Setting pipeline to PAUSED ...
Pipeline is live and does not need PREROLL ...
Setting pipeline to PLAYING ...
New clock: GstSystemClock
^Chandling interrupt.
Interrupt: Stopping pipeline ...
Execution ended after 0:00:03.837059981
Setting pipeline to PAUSED ...
Setting pipeline to READY ...
Setting pipeline to NULL ...
Freeing pipeline ...
nvidia@jetson-0420119049088:~$
```

9. To end the streaming process, press **Ctrl** + **C** on the keyboard.
10. Enter the following command line to switch or change the parameters of the specific camera (1, 2, 3, or 4 respectively.

    `device=/dev/video0 to 1,2,3,4.`

All camera streams can be viewed simultaneously using the integrated multi-camera features within the built-in application.

11. Enter the following command line to view all camera streams simultaneously within the terminal.

    `./e-multicam.elf`

17.3 Serial Multiprotocol Configuration

Elton baseboard is equipped with four serial ports routed from the AGX Xavier Series Module through the programmable SP336 serial transceiver and implement selected RS232/422/485 protocols via GPIOs.

The SP336 is an integrated multiprotocol serial transceiver that contains both RS-232 and RS-485/RS-422 receivers and drivers and can be configured to operate in eight modes including RS-232-only (4Tx/4Rx), RS-485/RS-422-only (2Tx/2Rx) full or half-duplex, two RS-232/RS-485/RS-422 mixed-modes.

When configured in RS-485/RS-422 mode, each driver can be individually enabled for use on shared buses or bidirectional communication.

The SAM D51 microcontroller utility controls all four ports on the SP336 transceiver.

The microcontroller utility is used to set the modes for Ports 1 and 2 and the platform GPIOs are used to set the mode for Ports 3 and 4.

Launch the SAM microcontroller utility and set the mode as depicted in the screen below.

```
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$ sudo ./DSCSAM_SerialPortConfig
[sudo] password for nvidia:
Board Type : ELTON

 DSC SAM SERIAL PORT CONFIGURATION DEMO
Enter Serial Port Mode (0-RS232,1-RS422, 2-RS485):2
press Enter to repeat or 'q' to quit:q

DSC SAM Serial Port Configuration demo completed.
```

Figure 17.3-1: SAM Utility Serial Port Configuration

The RS485_util provides the option to enable or disable RS485/422 direction control on the UART ports.

NOTE: The RS485_util must be run after the ports are opened. Running the utility before the ports are open may result in the Terminal utility resetting the flag settings.

Before transmitting, set the mode for individual ports.by replacing the -n parameter with the port number as shown the syntax below.

```
#sudo rs485_util ttyTHS<n> 1
```

During transmission the RX protocol will be disabled. After the transmission is complete the RX protocol will be enabled as depicted in the syntax and screen below.

```
#sudo rs485_util ttyTHS<n> 0
```

```
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$ sudo rs485_util ttyTHS0 1
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$
nvidia@jetson-0420119049088:~/Sam_Linux_64bit_CLI_Demos/DSCSAM_SerialPortConfig$ sudo rs485_util ttyTHS0 0
```

Figure 17.3-2: Enabled RX Protocol Screen

The table below lists the GPIO values and transceiver modes.

Sysfs GPIO Number	*RS232*	*RS422*	*RS485*
443	1	1	0
444	0	1	1

17.4 CAN Controller Configuration

The AGX Xavier Series Module integrate two independent CAN ports/channels which support connectivity to two CAN networks. The CAN interfaces can0 and can1 are routed to the Elton baseboard via CAN busses. The maximum speed that is supported is 1 mbps.

The CAN network driver provides a generic interface to setup, configure, and monitor CAN devices. The program ip is used to configure bit-timing parameters.

The following command line invokes the IP link to set the CAN bus bitrate before all operations begin.

```
sudo ip link set can0 type can bitrate 1000000
```

The following command line toggles the link up or down.

```
sudo ip link set up can0
```

The following command line sends CAN-frames via CAN_RAW sockets.

```
cansend can0 5A1#1122334455667788
```

The command candump dumps traffic on a CAN network The following syntax shows the message received from the CAN bus.

```
candump can0
```

18. LIMITED WARRANTY POLICY

Diamond Systems Corporation warrants that its products will be free from defects and errors in material and workmanship and perform in full accordance with the technical specifications stated in the description of the product for a 2-Year Period from the Date of Shipment.

Unless otherwise stated, Diamond Systems Corporation Limited Warranty Policy covers the following criterion:

- It is extended to the original Purchaser/Consumer.
- Under Terms and Conditions of the Warranty, Diamond Systems Corporation, at its sole discretion, will repair or replace any defective parts or components of its product.
- The product must be returned to Diamond Systems Corporation in the-approved packaging, pre-authorized with a Diamond Systems Corporation-assigned Return Material Authorization (RMA) Number which is referenced on the shipping document.
- The Customer will prepay the shipment cost of the product to the Diamond Systems Corporation designated site.
- Diamond Systems Corporation will prepay the return shipping cost of the repaired or replaced the RMA product.

Diamond Systems Corporation Limited Warranty Policy does not cover product defects or damages incurred due to:

- Attempts by Customer to repair or resolve any product issues without the prior consent of Diamond Systems Corporation.
- Mishandling, misuse, neglect, normal wear, and tear, or accident.
- DIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES RESULTING FROM ANY BREACH OF WARRANTY OR CONDITION, OR UNDER ANY OTHER LEGAL THEORY, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DOWNTIME, GOODWILL, DAMAGE TO OR REPLACEMENT OF EQUIPMENT AND PROPERTY, ANY COSTS OF RECOVERING, REPROGRAMMING, OR REPRODUCING ANY PROGRAM OR DATA STORED IN OR USED WITH DIAMOND SYSTEMS CORPORATION PRODUCTS, AND ANY FAILURE TO MAINTAIN THE CONFIDENTIALITY OF DATA STORED ON THE PRODUCT.

NOTE: THE LIMITED WARRANTY POLICY DOES NOT WARRANT TO REPAIR ANY OR EVERY DIAMOND SYSTEMS CORPORATION PRODUCT.